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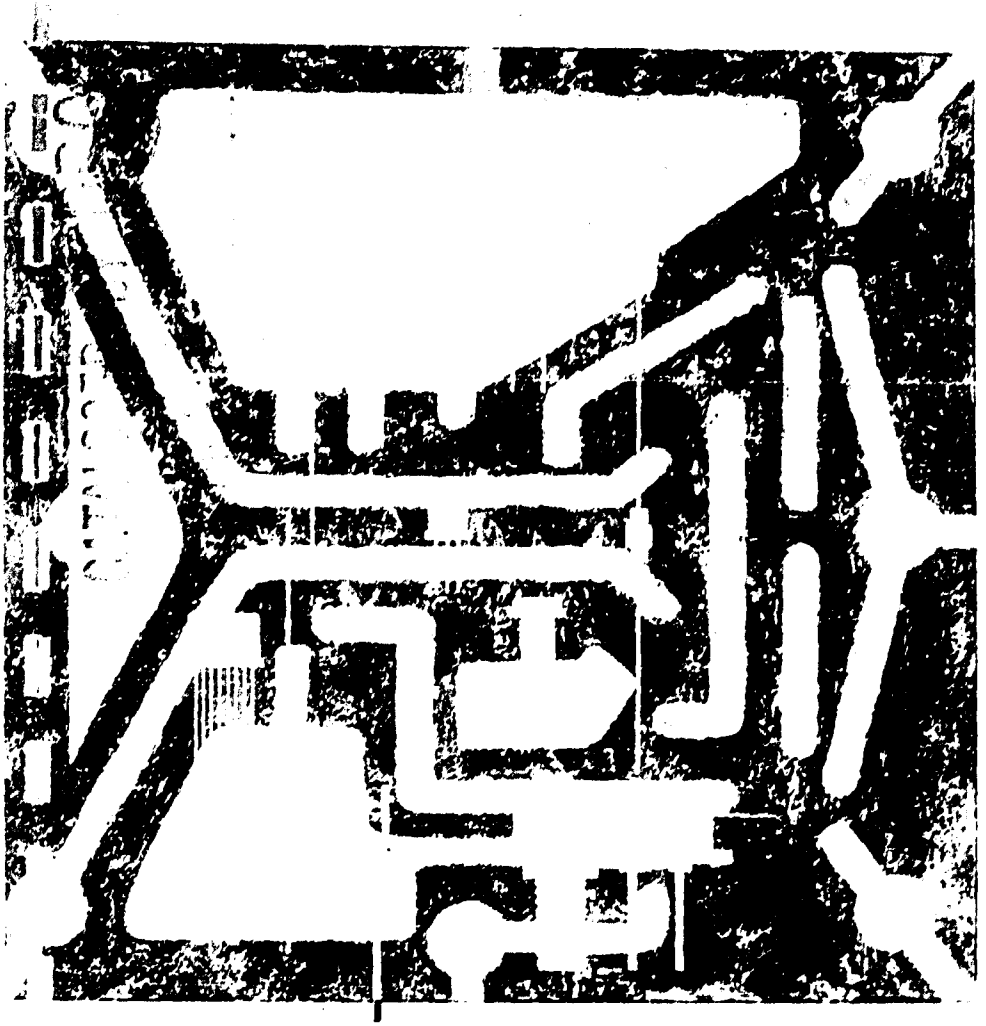


PRODUCTION ENGINEERING MEASURE

Transistor, VHF, Silicon, Power
(75)

FOURTH QUARTERLY REPORT

1 April 1963
to
30 June 1963

PSI Report No 3000:47-Q-4

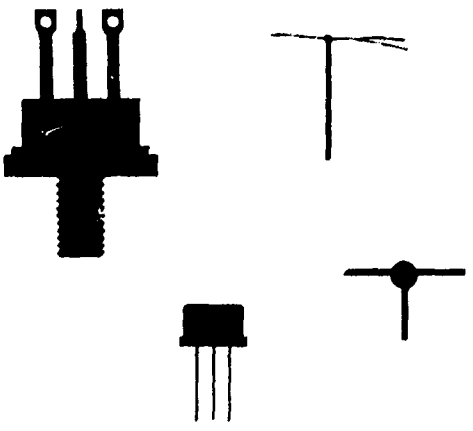
Prepared By

R. N. Clarke
J. W. Ewins
R. C. Neville

Edited By

J. Durst

U.S. Army Electronics Materiel Agency
Contract No. DA 36-039 SC-86733
Order No. 19055-PP-62-81-81



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FOURTH QUARTERLY REPORT

PRODUCTION ENGINEERING MEASURE

Transistor, VHF, Silicon, Power (75W)

1 April 1963 to 30 June 1963

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U.S. Army Electronics Materiel Agency
Contract No. DA 36-039 SC-86733
Order No. 19055-PP-62-81-81

This contract calls for the establishment of a limited production facility, the delivery of 2,475 25-watt, 100-megacycle transistors, and a study of the requirements for beginning a large scale production operation.

Prepared By

R. N. Clarke, J. W. Ewins, R. C. Neville

Edited By

J. Durst

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SECTION I - ABSTRACT

Delivery of the third group of "state-of-the-art" devices was made during the period covered by this report. The accumulative total of these shipments is 225 units.

The primary considerations of this report are the design analysis of the present DPT 685 devices, and an alternate design oriented toward alleviating power dissipation problems, as related to second breakdown phenomena, and toward frequency performance.

The balance of the report is concerned with the N type diffusion improvement, the introduction of the 11/16 Coldweld Copper-Ceramic Package, and the electrical performance of the existing DPT 685 supplemented by a series of curves.

SECTION II - PURPOSE

The terms of the contract require the contractor to establish a limited production facility using prototype equipment capable of producing parts directed toward a rate of 200 transistors, that meet the applicable specifications, per eight hour shift. During the contract period, the contractor shall deliver a total of 2,475 transistors, of which 375 are to be engineering samples, 100 are to be pre-production samples, and 2,000 are to be pilot production devices. The 2,000 transistors produced during the pilot line run shall meet the applicable technical specifications. The specifications include performance as an amplifier - the transistor must be capable of 25 watts of power output at 100 megacycles with 10 db of power gain - and as an oscillator - the transistor must deliver 25 watts at a frequency of 100 megacycles. In addition, the package must be such that the transistor is electrically isolated from the case.

The prototype equipment required for the establishment of the pilot production run will be developed and supplied at the expense of the contractor.

Upon completion of the pilot production run, a Step II Study will be made to determine the requirements of a manufacturing facility capable of producing 50,000 units per month, meeting the applicable technical specifications and based on one eight hour shift per day. The necessary plans and schedules required to establish the production capability, based upon equipment capacity and pilot production yields, shall be incorporated in the Step II Study.

SECTION III - TECHNICAL DISCUSSION

Chapter 1

Introduction

The following two chapters in this section contain the essence of this report. A thorough review of the processing changes, progress, and problems encountered during the period of interest is made. The Electrical Characterization carried out on the DPT 685 during the period of interest is reviewed and two points made clear:

1. The device is optimized, performance wise, about its bias level (80 volts, 600 ma), and

2. The required power dissipation level exceeds the present day second breakdown locus.

It is for the above reasons that the design work in Chapter 2, Paragraph 2, was done. There it is shown that in order to reduce the thermal resistance to an adequate level, it is necessary to increase by some 50% the emitter stripe length. Using this as a starting point, the required device design for the bias level (70 volts at a suggested 60 watts) is derived. It is shown that the design is adequate insofar as frequency performance is concerned. The problem involved is a high voltage (70 volts) and possible attendant thermal run-away problems:

1. The second breakdown problem is associated with the amount of energy stored in, and dissipated by, a transistor. The higher

the operating voltage level, the greater the problem with second breakdown.

2. A change from 80 volts - the present level of bias - to 70 volts is minor, but a possible change to 25 volts would involve a substantial modification of the processing sequence. On the other hand, studies of potential Military use show that the 25 volt capability is preferable due to the consequent freedom from voltage converters in field equipment.

Chapter 2

Device and Process Engineering

2.1 Introduction

A comparison of two possible designs for the 75 Watt-PEM transistor has been made. Calculations show that the current device, produced under Contract No. DA 36-039 SC-86733, is marginal as designed. A series of devices which would perform as desired are derived in Paragraph 1 . In particular, two devices are explored. A transistor biased at 70 volts and 715 ma is shown to be acceptable, but susceptible to second breakdown failures. The other device is the current DPT 685 transistor.

Substantial progress has been made in diffusion. The principal improvement for the quarter was the replacement of P_2O_5 as a source for n-type dopant, by $POCl_3$ on all n-type diffusions. A new collector-contact diffusion, also featuring $POCl_3$, was designed and put into operation.

The package processing section reviews the program under progress and gives drawings detailing the new 11/16 Coldweld Copper-Ceramic Package.

2.2 Device Design

Over a period of seven years, Pacific Semiconductors, Inc., has evolved a relatively simple first order design theory which combines the theoretical knowledge of the designer with a backlog of empirical information which is also readily available within the company.

In any design, one finds a set of often conflicting requirements which serve to limit the degree of freedom available to the designer. In particular, the requirements of high power and high frequency are conflicting. High power historically demands a large area to dissipate the resultant heat, while high frequency demands a small area with its resultant low capacitance. The designs to follow illustrate these problems and do so in what is hoped is sufficient detail to enable the reader to determine for himself the difficulties to be encountered in making any given alteration in device parameter.

The results of the design work presented in this paragraph are given in the following two tables. Table 2.2.1 shows the physical designs and provides evidence that the designs are adequate from a frequency viewpoint. Table 2.2.2 shows some of the pertinent electrical characteristics which a device would have under the designs in Table 2.2.1. The two designs presented are:

1. The current design, optimized at a bias level of 600 mA and 80 volts, and which is known to be inadequate for reasons of thermal dissipation.

2. A design optimized at 715 mA and 70 volts, which is called out in SCS-129.

The reader is referenced to the bulk of this paragraph for a more detailed insight into the design theory used and to Table 2.2.3 at the end of this paragraph for clarification of the symbols used.

TABLE 2.2.1

Design Comparison

Parameter	Units	Current Design of DPT 685 "V"	70 Volt Design for Transistor "V_1"
A. Geometry			
Base stripe/emitter stripe ratio[2]		1	.6
Emitter stripe width, s	μ	90	90
Emitter geometry[1]	μ	20μ-50μ-20μ	18μ-54μ-18μ
Base geometry[1]	μ	20μ-50μ-20μ	18μ-18μ-18μ
Stripe length, L	cm	1.0	1.56
Emitter area, A_e	cmμ	90	140.4
Collector area, A_c	cmμ	270	309
B. Vertical Dimensions			
Emitter depth, d_e	μ	1.8	1.8
Base depth, d_b	μ	2.6	2.6
Base width, W_b	μ	0.8	0.8
Collector width, W_c	μ	22	19
Dice width, W_D	μ	126	123
C. Collector Region			
Resistivity, ρ_c	ohm-cm	13 ± 2	11 ± 1
n-concentration, N_c	$/cm^3$	6×10^{14}	7×10^{14}

1. Silicon-metal-silicon.

2. The ratio of the width of 1/2 of the difference between the widths of the emitter-base and collector-base junctions to that of the emitter-base junction.

TABLE 2.2.1 (Continued)

Design Comparison

Parameter	Units	Current Design of DPT 685 "V"	70 Volt Design for Transistor "V_1"
C. Collector Region (Continued)			
Depletion width, $w_c(V)$			
at V = V (bias)[2]	μ	13.3	11.5
at V = V (breakdown)[2]	μ	19.4	16.8
Capacitance per area, C_c/A_c			
at V = V (bias)[2]	pfd/cmμ	.08	.093
Capacitance, C_c			
at V = V (bias)[2]	pfd	21.6	28.7
Current density			
J(=)	amps/cm^2	577	672
J max[3]	amps/cm^2	167	107
J (operating)	amps/cm^2	67	50.9
D. Base Cutoff Frequency[4]			
Parasitic Resistance r'_b	ohms	.026s/L	.022 s/L
r'_b	ohms	2.34	1.27
Frequency f_b	cps	3.62 X 10^9	4.37 X 10^9

2. Refer to Table 2.2.2

3. J max = I maximum/A_e

4. Hereafter, s in μ, L in cm

TABLE 2.2.1 (Continued)

Design Comparison

Parameter		Units	Current Design of DPT 685 "V"	70 Volt Design for Transistor "V_1"
E. Emitter Cutoff Frequency				
Emitter Diffusion Resistance	r_e		.051	.040
Capacitance per area	C_{Te}/A_e	pfd/cmμ	26.8	26.8
Capacitance per area	C_{Te}	pfd	2412	3762
	f_e	cps	1.29×10^9	1.06×10^9
F. Collector Cutoff Frequency				
Collector Parasitic Resistance	r'_c	ohms	113/sL	82.5/sL
	r'_c	ohms	1.26	.586
Emitter Parasitic Resistance	r'_e	ohms	1.42/sL	1.42/sL
	r'_e	ohms	.0158	.0101
	f_c	cps	5.56×10^9	8.7×10^9
G. Alpha Cutoff Frequency	f_a	cps	6.13×10^8	6.51×10^8
H.	f_T	cps	384×10^6	384×10^6
I. Figure of Merit	$G_p f^2$	cps^2	35×10^{16}	42.2×10^{16}

TABLE 2.2.1 (Continued)

Design Comparison

Parameter		Units	Current Design of DPT 685 "V"	70 Volt Design for Transistor "V_1"
J. Power Gain (G_p) (f = 100mc)		-	35	42.2
		db	15.4	16.2
Less 3 db for large signal operation		db	12.4	13.2

TABLE 2.2.2

Probable Electrical Characteristics

Parameter	Units	80 Volt-600ma Design "V"	70 Volt-715ma Design "V_1"
A. Bias Level			
Collector Current	ma	600	715
Collector Voltage	volts	80	70
B. DC Conditions			
BV_{CBO} (I_c = 5ma)	volts	170	150
BV_{CES} (I_c = 5ma)	volts	170	150
BV_{EBO} (I_E = 5 ma)	volts	5	5
Maximum Power Dissipation (I_c, V_{CE} at bias level) I_c = 25°C	watts	25[1]	75[2]
Maximum Current	amperes	1.5	1.5
C. Frequency Performance			
Power Gain (I_c, V_{CE} at bias P_{in} = 2.5 watts f = 100MC $T_L \leq 55°C$	db	>10	>10

1. Actual.
2. Specified by SCS-129.

TABLE 2.2.2 (Continued)

Probable Electrical Characteristics

Parameter	Units	80 Volt-600ma Design "V"	70 Volt-715ma Design "V_1"
D. Other			
Capacitance	pfd	≤ 25	≤ 30

Generalized Line Structure

In Figure 2.2.2 is shown the general plan and cross section view of a generalized transistor.

The analysis of a transistor operating at high frequency indicates that the performance is limited by the combination of various resistance-capacitance time constants and the delay time required for carriers to move from emitter to collector. For a given thickness, the carrier transit time is invarient with width and length of the transistor. The width of the active region is responsible for determining the resistance-capacitance product, while it is independent of the thickness and nearly so of the length. In fact, it is so nearly independent of length that we ignore this dependence in our first order theory. Therefore, to a very close approximation the transistor can be specified, as to frequency, by considering only the width and thickness of the active region.

The power requirements of a transistor dictate the length required. For a given length, a given current can be made to pass through the transistor and a given amount of power dissipated. It is the power dissipation problem which is primarily responsible for the redesign of the 25W-100MC transistor (DPT 685) to qualify it for the rigorous power requirements of Contract NO. DA 36-039 SC-86733. Therefore, the required power rating specifies the minimum length of the transistor.

Thus, "width" and "thickness" are used to satisfy the frequency requirement and "length" is used to meet power demands.

In Figure 2.2.1 we have an equivalent circuit for use with these transistors.[1] Considering the transistor to operate as an amplifier with a lossless feedback, βK, to cancel the internal feedback, one finds as below:

a. $G_p f^2 = \frac{f_b f_t}{4}$

b. $f_t^{-1} = f_a^{-1} + f_e^{-1} + f_c^{-1}$

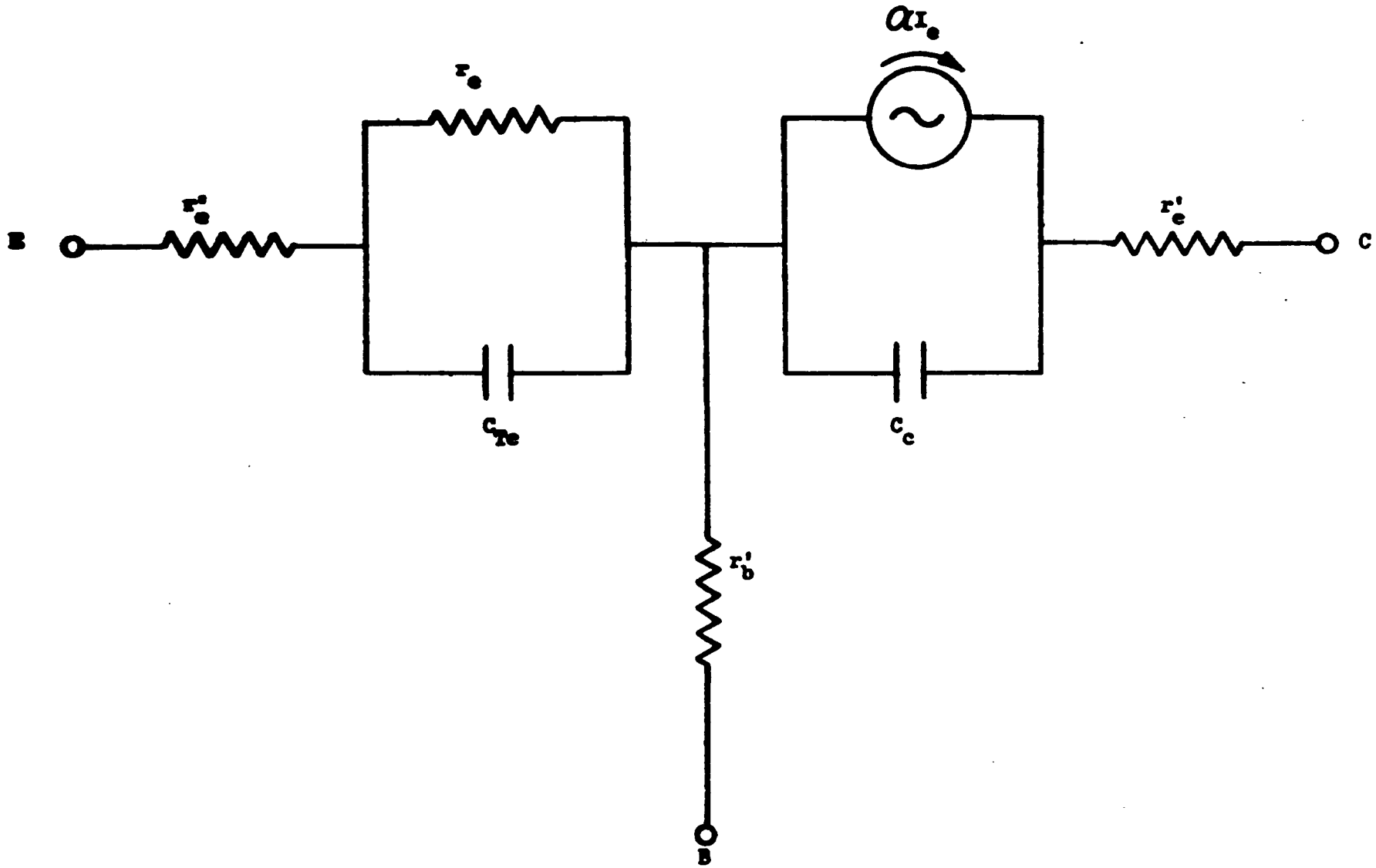
c. $f_b^{-1} = 2\pi r_b' C_C$

d. $f_e^{-1} = 2\pi r_e C_{Te}$

e. $f_c^{-1} = 2\pi C_C (r_e' + r_c' + r_e)$

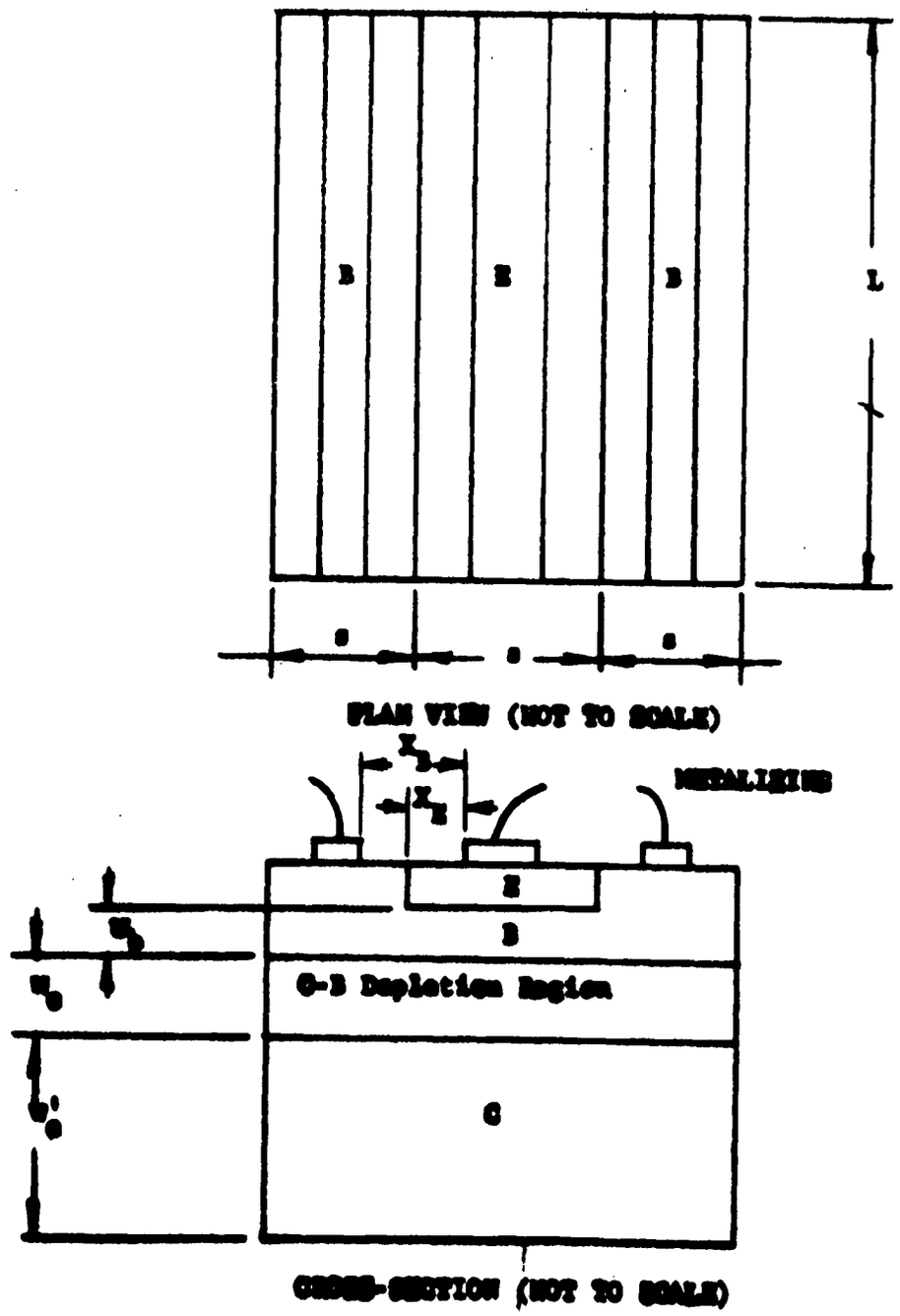
f. $f_a = \frac{1.2 Dn}{\pi W_b^2} \left(1 + \frac{1.2 Dn}{\pi W_B^2} \frac{\pi W_c}{V_T}\right)^{-1}$

1. The reader is referenced to the end of this paragraph for a definition of terms.



TRANSISTOR EQUIVALENT CIRCUIT

Figure 2.2.1



BASIC LINEAR TRANSISTOR STRUCTURE

Figure 2.2.2

Approach

This theory will be used in the following sections to derive a design for the 75 watt-PEM transistor. In point of fact, two transistors will be designed:

1. The design of the current device (DPT 685) will be derived in detail and it will be shown that this design is not adequate to the task assigned it.

2. A seventy (70) volt operating-bias device will be designed which performs with the desired power output at the desired frequency.

These two designs can be compared and contrasted with one-another to further illuminate the problems encountered in such a design.

Thermal Design

One of the basic problems inherent in the original design of the DPT 685 was the thermal resistance problem. It is well to attack this problem first.

The DPT 685 has, at present, a thermal resistance (measured at four watts dissipation with a case temperature of 25°C) of:

1. $\theta_{RJC}(25^{\circ}C) = 2.3^{\circ}C/watt$

From manufacturers data[1] the thermal resistance of beryllia oxide

---

1. National Beryllia Corporation, Haskell, New Jersey

at 200°C is one and one-half times that at 25°C. This means that:

2. $\theta_{RJC}(200^{\circ}C) = 1.5\ \theta_{RJC}(25^{\circ}C)$

$= 3.45^{\circ}C/watt$

Provided that we assume θ vs T curve for silicon similar to that for beryllium oxide.

The required maximum power dissipation requirement for the transistor under SCS-129 of 12 February 1962 is:

3. $P_d = 75$ watts (with a case temperature of 25°C)

Using equations Number 2 and 3 we obtain for the junction temperature:

4. $T_J = 25 + 75\ (3.45) = 285^{\circ}C$

This value is too high for comfort. When one looks at curves[1] of resistivity versus temperatures, that point at which resistivity drops radically appears to be in the neighborhood of 500°C depending on the exact resistivity used. The lower this resistivity, the higher the trigger temperature. The approach here will be to restrict the temperature of the junction while using the minimum value of resistivity. The 70 volt design best meets this requirement.

As an absolute minimum, the transistor must be capable of dissipating 50 watts, which can occur in the no-drive operating condition.

---

1. Pearson and Bardeen, "Physics Review", 75, p. 865 - 883, 1949

By taking a maximum junction temperature of 200°C and calculating for θ_{RJC}:

5. $\theta_{RJC} = \frac{200 - 25}{75}$

$= 2.5°C/watt \text{ at } 200°C$

Therefore:

6. $\theta_R = 1.67°C/watt \text{ at } 25°C$

For conservative design, and to assure a high yield process, we set θ_{RJC} to be:

7. $\theta_{RJC} = 1.5°C/watt \text{ at } 25°C$

It is possible to compute the approximate thermal resistance of a transistor knowing the properties of the materials used in its construction (silicon, beryllium oxide, molybdenum, etc.) and the critical regions where heat is generated in the device (the base-collector junction under the emitter). Possible, but not very practical. The properties of the ten-to-fifteen interfaces in the heat path between junction and case are computationally uncertain quantities and the variation from device to device is too great. However, empirical expressions can be generated and, at PSI, a value for such an empirically derived junction-case thermal resistance has been generated. This value has been checked on both the 5W-70MC (Contract No. DA 36-039 SC-85960) and the 25W-100MC (Contract No. DA 36-039 SC-87342) transistors. These devices both employ beryllium oxide isolating tabs and are similar in design to the 75 watt transistor. The relation is:

8. $\theta_R = \frac{210}{sL}$ (s in μ, L in cm, θ_R in $^{\circ}C$/watt)

Using equations Number 8 and 7, we arrive at:

9. $sL = 140$ cmμ

The value of s is determined from the frequency design and this leaves us with a minimum value for L, the equivalent stripe length of:

10. $L = \frac{140}{s}$ cm

Collector Region Design

The collector region design is dictated by a number of factors. It is usually easier to start the analysis with a look at the base-collector breakdown and a determination of the minimum resistivity needed to support this. This is to be followed with an analysis of the current carrying capability of the collector-base space charge capacitance. As stated before, we shall design the transistor for two separate operating voltages, simultaneously.

A. Collector-Base Breakdown

A.1 The 25W-100MC transistor currently in production. (To be designated hereafter as the "V".)

11. V_{CE} (bias level) = 80 volts

Therefore:

12. BV_{CBO} = 170 volts

and, from experience:

13. $\rho_c = 13 \pm 2$ ohm-cm

14. $N_c = 6 \times 10^{14}/cm^3$

A.2 The 70 volt bias level transistor. (To be designated hereafter as the V_1".)

15. V_{CE}(bias level) = 70 volts

therefore:

16. $BV_{CBO} = 150$ volts

and, from experience:

17. $\rho_c = 11 \pm 1$ ohm-cm

18. $N_c = 7 \times 10^{14}/cm^3$

B. Collector-Base Space Charge Width

The collector-base junction is, to a good approximation, quite abrupt. As a result, the collector-base space charge region extends mostly into the collector region. By taking an abrupt junction profile, and using Poisson's equation, we arrive at:

19. $W_C = (2\epsilon V_{CB}/q N_c)^{1/2}$

Where the terms are defined in the appendix, at the end of this section:

B.1 The "V" version (80 volts bias level)

20. a. w_c (80) = 13.3 μ

b. w_c (170) = 19.4 μ

B.2 The "V_1" version (70 volts bias level)

21. a. w_c (70) = 11.5 μ

b. w_c (150) = 16.8 μ

C. Using equations Number 24 through 26, we can determine the minimum width for the high-resistivity portion of the collector region based on supporting the required breakdown voltage and on knowledge of processing tolerances available to the designer.

C.1 For the "V" version:

The process being used currently results in a collector region width, W_C, of:

22. $W_C = 22 \pm 2.5\ \mu$

C.2 For good design, we put for the "V_1" modification:

23. $W_C = 19 \pm 2.0\ \mu$

D. Space Charge Region Current Capacity

Following the work of Ryder, we can estimate the maximum amount of current which can be put through the base-collector space charge region without adversely affecting device performance. The problem is as follows.

There is a certain basic amount of fixed charge in the base-collector space charge region.

24. $Q_{fixed} = Q N_c w_C A_C$

There is also a quantity of charge in transit across this region by means of the drift mechanism.

25. $Q_{mobile} = \frac{J w_C A_C}{V_t}$

If the mobile charge begins to approximate the fixed charge in magnitude, several mechanisms begin to operate. In general:

A. The space charge region attempts to change dimension to continue supporting the voltage applied across it. The result is a decrease in base-carrier transit time.

B. Electrons in the base region see a negative charge in the collector-base space charge region and so are repelled, forcing a large surge of base current.

The results are:

a. A fall off in gain.

b. An increase in r'_c.

c. A rush of current out the base lead, which is frequency fatal to the device.

The designer can combat this by utilizing either of two defenses. He can increase the overall active area and so decrease the current density, or he can lower the resistivity and increase the fixed charge present. A useful figure of merit in these cases is J equivalent $\equiv$ J(=). This parameter is found by setting the mobile and fixed charges equal and solving for J.

26. $J(=) = q N_c V_t$

The values of J, most easily determinable for any transistor, are those of its operating current, J(op), and maximum current, J(max). These quantities, together with J(=), are reproduced below for the assumption of uniform flow across the emitter-base junction:

D.1 For the "V" version:

27. a. $J(=) = 577 \text{ amps/cm}^2$

b. $J(op) = 6000/sL$ amps (s in μ, L in cm)

c. $J(max) = 15000/sL$ amps (s in μ, L in cm)

D.2 For the "V_1" version:

28. a. $J(=) = 672 \text{ amps/cm}^2$

b. $J(op) = 7150/sL$ amps (s in μ, L in cm)

c. $J(max) = 15000/sL$ amps (s in μ, L in cm)

E. Collector-Base Capacitance

The next item of business is the collector-base capabitance. This calculation is not so straight forward as it might seem at first glance. The desired signal does not see the collector capacitance in its entirety. That portion of the collector-base space charge region which does see the signal lies almost directly beneath the emitter. The collector capacitance is then made up of two components; one of which is in the signal path and another which is parallel and theoretically tunable. However, it appears that good practice dictates that we consider the entire capacitance as the effective capacitor.

For an abrupt junction, the capacitance per unit area is:

29. $C = (q \epsilon N_c/2\ V)^{1/2}$

30. C_C = Full collector capacitance
$= A_C (q \epsilon N_c/2\ V)^{1/2}$

The capacitance desired is that at the operating bias.

E.1 Capacity for "V" version:

31. $C_C = A_C$ (.08 pfds/cm μ)

E.2 Capacity for "V_1" version:

32. $C_C = A_C$ (.093 pfd/cm μ)

Frequency Design

It is now possible to proceed with the design of the DPT 685 as a high frequency transistor. We need one additional piece of information before we can gain real insight into the problem, however. Our knowledge about the physical device must include information about the emitter and base regions to allow a complete calculation. A single set of parameters for these regions will be used for the versions of the DPT 685 under consideration:

33. Emitter depth, D_e, 1.8 μ
34. Base depth, D_b, 2.6 μ

} Assumed for good engineering practice.

leading to:

35. Base width, W_b, .8 μ

A. Base Cutoff Frequency

This parameter results from the charging process of charging the base-collector capacitor through the base parasitic resistance. One can write for this parameter, after the introduction:

36. $$f_b^{-1} = 2 \pi r_b' C$$

The value to use for C_C is that value of collector capacitance which is actually seen by the signal, which corresponds to that under the base region. This quantity was derived in equations 31 and 32 for the two versions under consideration.

To derive the expression for base parameter resistance, reference is made to Figure 2.2.2. From this it appears that we can write for r'_b:

$$37.\quad r'_b = 1/2 \left(\frac{X_B}{L} R_{SB} + \frac{X'_E}{L} R'_{SB} \right) \quad (1)$$

From past experience, we have found that one can put for X_B and X'_E:

$$38.\quad X'_E = s/3$$

$$X_B = \frac{A_C - s}{6}$$

We have for R_{SB} and R'_{SB}:

$$39.\quad R_{SB} = 100\ \Omega/\square$$

$$R'_{SB} = 1260\ \Omega/\square$$

To compute A_c we must make some assumptions. Normally, the base region on either side of the emitter is of the same width as the emitter. However, this need not be so. In fact, since the emitter must carry the greatest current, it becomes useful to have the emitter larger than either one of the two base regions. We have chosen the following configurations for the two versions under consideration:

a. For the "V" version:

Emitter width s

Base width s (on one side)

Collector width 3s

---

1. This expression is the parallel sum of two resistances - each composed of two resistors in series.

b. For the "V_1" version:

Emitter width s

Base width .6s (on one side)

Collector width 2.2s

Therefore, we have for r_b':

For the "V" version:

40. a. $r_b' = .0226\ s/L$ (s in μ, L in cm)

For the "V_1" version:

40. b. $r_b' = .022\ s/L$ (s in μ, L in cm)

From equations Number 31, 32, 36 and 40 we can now compute the base cutoff frequency:

41. $f_b^{-1} = 2\pi r_b' C_1$

or, for the "V" version:

42. a. $f_b^{-1} = 341.4 \times 10^{-16}/s^2$

b. $f_b = 2.93 \times 10^{13}/s^2$ cps

and, for the "V_1" version:

43. a. $f_b^{-1} = 2.83 \times 10^{-14}/s^2$

b. $f_b = 3.53 \times 10^{13}/s^2$ cps

B. Emitter Cutoff Frequency

This parameter in the high frequency analysis comes to pass as a result of the process involving the charging of the emitter-base capacitor through the emitter diffusion resistance.

The expression for this quantity is:

$$44. \quad f_e = (2 \pi r_e C_{Te})^{-1}$$

The emitter resistance is determined from the well known expression:

$$45. \quad r_e = KT/q \, I_E$$

The barrier capacitance of the base emitter junction is difficult to compute. The emitter-base junction is biased in the forward direction during operation. This results in a very small effective voltage across the junction. Since the junction is formed by the superposition of an n-type on a p-type diffusion, and, as a result of the low bias level on the junction, the emitter barrier capacitance has the form of a graded junction capacitance. Furthermore, one can pick for the actual potential across the junction, $\psi - V_{BE} = 0.2$ volts, and be assured of the accuracy of solution since the variation in barrier capacitance as $\psi - V_{BE}$ across the zero line is very small. The emitter-base capacitance is therefore governed by the expression:

46. $C_{Te} = \frac{\epsilon}{2} \left[2\, qd/3\epsilon\, (\psi - V_{BE}) \right]^{1/3} sL$

where: $\psi - V_{BE} = 0.2$ volts.

The slope d is the same for both designs since we have fixed the base and emitter diffusions to be almost identical in both versions.

47. $d = 2.58 \times 10^{31}/m^4$

Therefore, bearing in mind that s and L are different for each modification, the barrier-capacitance for both designs is:

48. $C_{Te}/sL = 26.8$ pfd/cm μ

Using equation Number 45, we find for the emitter resistance:

For the 80 volt design:

49. a. $T = 355^{o}K$

50. a. $r_e = .051$ ohms

For the 70 volt, "V_1", design:

49. b. $T = 335^{o}K$

50. b. $r_e = .040$ ohms

Putting equations Number 44, 48 and 50 together for the "V" design:

51. a. $f_e^{-1} = 8.58 \times 10^{-12}\, sL$

b. $f_e = 1.17 \times 10^{11}/sL$ cps

For the "V_1" design:

52. a. $f_e^{-1} = 6.74 \times 10^{12}$ sL

b. $f_e = 1.48 \times 10^{11}/sL$ cps

C. Collector Cutoff Frequency

The parameter arises as a result of charging the base-collector capacitor by way of the emitter-collector-resistance. For this item one can write:

53. $f_c = 2\pi \, (r_e + r'_e + r'_c)^{-1}$

The collector-base capacitance is that seen by the radio frequency signal and hence is the capacitance derived earlier as equations Number 31 and 32.

The emitter diffusion resistance was derived in equation Number 50.

The parasitic resistances r'_e and r'_c remain to be derived here.

The collector parasitic resistance arises mostly from the high resistivity, non-depleted collector region. Almost no effect is seen from a well designed collector contact. As a result, one can put:

54. $r'_c = \rho_c \left[\frac{W_c - w_c \text{ (bias level)}}{A_e} \right]$

Using equation Number 54, and putting in values from equations Number 13, 17, 20 and 21, one can find:

For the "V" design:

55. $r'_c = 113/sL$ (s in μ, L in cm)

For the "V_1" design:

56. $r'_c = 82.5/sL$ (s in μ, L in cm)

where s and L vary for each design.

Considering the emitter parasitic resistance, one finds a considerably more difficult problem. There are essentially three factors which affect the emitter parasitic resistance:

1. The bulk resistance of the emitter silicon, which is quite low.

2. The bulk resistance of the lead wires and stripes on the silicon, which is low but appreciable.

3. The variable resistance resulting from the metallic interface of the silicon and metallizing.

The last factor is usually small and of the order of the metallizing resistance; or so large as to render the device inoperable. An empirical expression has been derived at PSI which adequately expresses the emitter parasitic resistance for a well constructed transistor:

57. $r_e' = 1.42/sL$ (s in μ, L in cm)

Knowing the required parameter, we are now in a position to calculate the collector cutoff frequency. Using equations Number 53, 55, 56, 57, 50, 31 and 32:

For the "V" design:

58. a. $f_c^{-1} = 1.510 \times 10^{-12}\ sL\ (.051 + 113/sL + 1.42/sL)$

b. $f_c^{-1} = 1.510 \times 10^{-12}\ sL\ \left(\frac{114.4}{sL} + .051\right)$

c. $f_c^{-1} =$ approximately 1.73×10^{-10}

59. $f_c = 5.78 \times 10^9$ cps

For the "V_1" (70 volt) design:

60. a. $f_c^{-1} = 1.283 \times 10^{-12}\ sL\ (.040 + 82.5/sL + 1.42/sL)$

b. $f_c^{-1} = 1.283 \times 10^{-12}\ sL\ (83.9/sL + .040)$

c. $f_c^{-1} =$ approximately 1.08×10^{-10}

61. $f_c = 9.25 \times 10^9$

There remains the calculation of signal delay time. Historically, this parameter limits the performance of a transistor more than any other. It is a function of the time required for carriers to drift and diffuse through the base and base-collector space-charge regions. The equation assumes that diffusion is the only mechanism effective in passing through the base region and that drift is the prime mechanism in the base-collector region.

One may write for this quantity:

$$62.\quad f_a = \frac{1.2\ D_n}{\pi\ W_B^2}\ \left(1 + \frac{1.2\ D_n}{\pi\ W_B^2}\ \frac{\pi\ W_C}{V_T}\right)^{-1}$$

Considering the base region, we have for the necessary quantities:

$$63.\quad D_n = 18\ cm^2/sec$$

$$W_B = .8\ \mu$$

Therefore, we have for both designs:

$$64.\quad \frac{1.2\ D_n}{\pi\ W_B^2} = 1.07 \times 10^9\ cps$$

There are variations which appear in the collector region due to the varying widths of the base-collector space charge region. Using equations Number 20 through 23:

For the 80 volt design at 80 volts:

$$65.\quad \frac{\pi\ w_C\ (V)}{V_T} = .696 \times 10^{-9}$$

For the 70 volt design at 70 volts:

$$66.\quad \frac{\pi\ w_C\ (V)}{V_T} = .602 \times 10^{-9}$$

Combining equations Number 62, 64, 65 and 66 one obtains:

For the "V" design"

$$67.\quad f_a = 6.13 \times 10^8\ cps$$

For the "V_1" design:

68. $f_a = 6.51 \times 10^8$ cps

D. High Frequency Performance

The designer is now in a position to write an expression for f_t and for the power gain bandwidth $G_p f^2$:

69. $f_t^{-1} = f_a^{-1} + f_e^{-1} + f_c^{-1}$

70. $G_p f^2 = f_b f_t/4$

Using equations Number 51, 52, 59, 60, 67 and 68 one obtains:

For the "V" design:

71. $f_t^{-1} = 1.63 \times 10^{-9} + 8.58 \times 10^{-12} sL + .173 \times 10^{-9}$

$f_t^{-1} = 1.83 \times 10^{-9} + 8.58 \times 10^{-12} sL$

For the "V_1" design:

72. $f_t^{-1} = 1.54 \times 10^{-9} + 6.74 \times 10^{-12} sL + .108 \times 10^{-9}$

$f_t^{-1} = 1.64 \times 10^{-9} + 6.74 \times 10^{-12} sL$

The value for power gain-frequency can now be calculated from equations Number 42 and 43, and 70 through 72:

For the "V" design:

73. a. $G_p f^2 = \dfrac{7.3 \times 10^{12}}{s^2 (1.83 \times 10^{-9} + 8.58 \times 10^{-12} sL)}$

For the "V_1" design:

74. a. $$G_p f^2 = \frac{8.8 \times 10^{12}}{s^2 (1.64 \times 10^{-9} + 6.74 \times 10^{-12} sL)}$$

The designer now takes the results of his thermal analysis, the device specifications, equations Number 73 a. or 74 a., and his knowledge of fabrication techniques, and choses values for s and L.

When these factors are all weighed one arrives at:

a. For the 80 volt design, which is already in existence, the following values were chosen:

1. $s = 90\ \mu$ = base and emitter width
2. $L = 1$ cm

This yields for figure of merit:

73. b. $G_p f^2 = 35.0 \times 10^{16}$

or, at a frequency of $f = 100 \times 10^6$, one hundred megacycles.

75. $G_p = 35.0$

$= 15.4$ db

Less 3 db for large signal operation:

76. $G_p = 12.4$ db

Since the present DPT 685 design is typically 10 db measured in the package and 11.0 db in the uncapped condition, we have:

Loss due to leads and header pins:

77. $-G_1 = 1.4$ db

Loss due to cap:

78. $-G_2 = 1.0$ db

b. For the 70 volt design, the designer arrives at:

1. $s = 90\ \mu$ = emitter stripe width
2. $.6s$ = base stripe width
3. $L = 1.56$ cm

The above combination leads to a thermal resistance of:

79. $\theta_{RJC}(25^{\circ}C) = 1.5^{\circ}C/watt$ (see equation Number 8)

This yields for figure of merit:

74. b. $G_P f^2 = 42.2 \times 10^{16}$

or, at a frequency of one hundred megacycles:

80. $G_P = 42.2$

$= 16.2$ db

less 3 db for large signal operation:

81. $G_P = 13.2$ db

General Remarks

The two designs which have been derived herein are summarized in Table 2.2.1 at the beginning of this Paragraph. The designs are adequate for the power and frequency, provided improved packaging can be found. The areas in which problems exist are those of thermal-resistance and second breakdown.

Insofar as thermal-resistance is concerned, the general increase in device length should assure trouble-free operation for the 70 volt design. It appears that the 80 volt transistor design upon which the thermal design equations are based is probably operating over perhaps only 75-90% of the emitter stripe. If this condition is rectified by better lead placement, as in the 70 volt design, then an improvement in thermal-resistance should insure more than sufficient heat dissipation to assure no problems with the design.

The second breakdown problem appears to be the most formidable. That this is a basic physical phenomenon, there can be no doubt. That the problem is accentuated by use of imperfect techniques and materials, there is also no doubt. This leads to an examination of the various approaches one can take to improve device performance in this aspect:

A. The higher the bias voltage in a transistor, the less the total power dissipation which that transistor can support. Thus, the lower the operating level, the more power can be pulsed through the device.

B. The lower the resistivity, the more uniform the silicon becomes. Even though the destruction of a device is finally accomplished through the negative temperature coefficient of silicon, a defect must exist to raise the temperature of a local spot to the required trigger temperature (250 - 350°C, depending on resistivity).

C. An increase in the level of technology would go a long way in the direction of improving tolerance to high power dissipations. Indeed, it is in this direction that the designer must go if significant improvements are to be made.

The conclusions then are:

1. The 80 volt bias level design is not capable of meeting the required performance level.

2. The 70 volt design involves improvements in technology sufficient to raise the second breakdown locus beyond its present level (see section on Electrical Testing).

3. A 25 volt design would involve a radical change in bias level which would result in essentially a brand-new transistor with challenging photoresist technology. The choice between the two electives is not an easy one to make, although the lower voltage is preferable from an end-use viewpoint. Not only is there a lower voltage

requirement for the equipment in the field making for lighter weight equipment, but there is a substantial reduction in vulnerability to second breakdown. Therefore, a significant portion of the work for the next quarter will be the analysis of such a low voltage device.

TABLE 2.2.3

Explanation of Symbols Used - In Alphabetical Order

A_c	Area of collector.
A_e	Area of emitter.
$C_c(V)$	Collector capacitance at a voltage V.
$C_{Te}(V)$	Emitter barrier capacitance.
d	Slope of impurity atom concentration at base-emitter junction.
D_b	Base diffusion depth.
D_e	Emitter diffusion depth.
D_n	Diffusion constant for electrons in base region.
ϵ	Permativity of silicon.
f	Frequency in cps.
f_a	Alpha cutoff frequency.
f_c	Collector cutoff frequency.
f_e	Emitter cutoff frequency.
f_t	$(f_a^{-1} + f_e^{-1} + f_c^{-1})^{-1}$
G_P	Power gain at a frequency f.
L	Emitter stripe length.
N_c	Impurity atom concentration on base region.
P_d	Power dissipation.
q	Absolute value of charge on electron.
r_b'	Base parasitic resistance.
r_c'	Collector parasitic resistance.
r_e	Emitter resistance.

TABLE 2.2.3 (continued)

r'_e	Emitter parasitic resistance.
R_{SB}	Base sheet resistance.
R'_{SB}	Base sheet resistance under emitter.
ρ_c	Resistivity of collector.
s	Emitter stripe width (see Figure 2).
T	Temperature in degrees Kelvin.
T_J	Junction temperature.
$\theta_{RJC}(T)$	Thermal resistance of a transistor, junction-to-case, at T degrees.
V_T	Scattering limited drift velocity.
W_B	Base region thickness.
W_C	Collector thickness.
$W_C(V)$	Base-collector space-charge region thickness.
X_B	Base current path length in base region not under emitter stripe.
X'_E	Base current path length under the emitter stripe.

2.3 Diffusion Processes

Diffusion operations are now in the final phase of the three phase program outlined and described in the Third Quarterly Report. The change of device design has not affected the validity of results obtained in phases I and II. The sequence of processing operations remains unchanged and the technique improvements introduced during phase II have made a smooth transition into phase III on the new design. The accumulated experience of the assigned personnel in performing the stabilized tasks of phase II results in constant processing techniques and the ability to quickly find the causes of problems and correct them. New furnaces will soon be operative, which will increase the control over diffusions, the capacity of the line, and the ease of processing. New photo resist alignment stations are being installed and improvements are being made on them to obtain faster and more accurate alignment of the patterns.

Phase I of the diffusion processes and supporting operations was a theoretical and practical diffusion set-up. Phase II consisted of technique improvement and controlled experimentation. Both of these phases were completed on the "V" parameter, DPT 685, pattern. All of the conclusions and processes developed during these two phases have made a natural transition into phase III, which is the establishment of a pilot line with well trained operators, the use of the best techniques acquired from phases I and II, and continued process improvement. The new transistor pattern, based on the V_1 design of Paragraph 2.2, has not required any major changes in the process

procedure. Photo resist advances, such as new ultraviolet light exposure systems, new alignment stations and Millipore filtering for photo resist application, are now all a part of the pilot line processes. Cleaning of wafers for diffusion is done in cascade ultrasonic systems, capable of measuring water conductivity. In addition to the $POCl_3$ emitter diffusion, a $POCl_3$ collector contact diffusion has also been developed and is now replacing the P_2O_5 dopant source.

The personnel assigned to the project have rapidly gained experience in performing their assigned tasks. These operators and supervisory personnel have had extensive semiconductor experience and consequently realize the importance, in phase III, of strict adherence to the processes, consisting of the best techniques developed in phases I and II. As a result, process variables because of untrained or unexperienced operators are minimized. This is especially important in photo resist and wafer cleaning prior to diffusion, where operator technique is an important part of any process. In addition, problems are recognized quickly, while they are still small, and the operators themselves often suggest the best solutions. The project is being further augmented in critical areas by the assignment of additional trained personnel and specialists.

Small furnaces, previously used on the pilot line, are being replaced with new, larger, long heat zone furnaces. As a result, there will be increased capacity through diffusions and close control over diffusion parameters. Control of these

parameters is essential because experience with the small, short heat zone furnaces shows that there is too much variation between diffusions and among the slices in each diffusion to permit the transistor being made with good yields. New wafer cleaning facilities are also being constructed. Sinks and cleaning stations are designed to avoid contamination from one wafer cleaning process to another. The new photo resist alignment stations are being equipped with stereo-metallurgical microscopes in order to provide the magnification and field-of-view necessary for accurate and rapid alignment of the patterns.

The Third Quarterly Report told of the reduction in contamination during N+ diffusions achieved by using phosphorus oxychloride rather than phosphorus pentoxide, and the development of a phosphorus oxychloride emitter diffusion. During the last quarter, a $POCl_3$ collector contact diffusion has been developed and is now replacing the old P_2O_5 procedures. The oxychloride collector contact process is reliable, easily controlled, cleaner, and run times, gas flows, and other variables are not extremely critical. Diffusion depths and collector sheet resistances are consistent from run to run. The furnace capacity through the two $POCl_3$ collector contact diffusions equals the capacity using previous P_2O_5 methods. In the oxychloride procedure, a five hour collector I diffusion is used for doping the slices. A large number of slices from several collector I diffusions are then stacked tightly together in the furnace for a five day collector II

diffusion. The resulting N+ diffusion depth of .004", and sheet resistances of .10 ohms/square, are identical to results obtained using P_2O_5. Plans for future processing call for exclusive use of phosphorus oxychloride collector contact diffusion.

The program for the next quarter is for continued work on phase III; which is the establishment of the pilot line using the best techniques acquired from the first two phases. Emphasis will be on making the pilot line operation a smooth, daily routine, capable of producing the transistors required by contract. Additional diffusion experiments are also planned. In particular, it is desired to optimize the methods for oxidizing silicon so as to grow oxides more consistent in thickness and color and, at the same time, obtain the highest possible collector-base reverse voltage breakdowns. This investigation will compliment, and will not interfere with, the basic objective. As already stated, this objective is the smooth, orderly operation of a pilot line, using the best techniques developed in phases I and II.

2.4 Packaging Processing

Few process changes were instituted during the period of this report as most of the effort was directed toward adaptation of existing processes for the use of the 11/16 Coldweld-Copper-Ceramic Package, and for the evaluation of the package itself. Search for the most versatile and yet production oriented assembly equipment has culminated, during this quarter, in the acquisition and check-out of most of the necessary equipment.

This section follows a general outline which can be given as follows:

Process Changes

Process Evaluations

11/16 Coldweld-Copper-Ceramic Package

Assembly Equipment

Process Changes

The use of the Copper-Ceramic Package has permitted improved techniques in beryllia tab brazing operations. The stud pins are supported by ceramic, thereby simplifying jigging and allowing more accurate location of beryllia tabs. Crystal to pin lead lengths are thereby shortened, resulting in lower input inductance.

Coldwelding techniques, initially developed on a previous contract (U.S.A.F. AF33(600)-43029), soon will enable a highly reliable hermetic seal to be achieved on the Copper-Ceramic Package.

As had been mentioned in the last (Third) Quarterly Report, a more sensitive hermetic leak check was being evaluated. During the period of this report, a Radiflow Leak Test was implemented to compliment the existing Glycerine Immersion Leak Test, which is most sensitive to gross leaks. The Radiflow Leak Test employs a radioactive gas bomb which, with the aid of an Isotope Rate Meter (Counter), can detect leaks as low as 10^{-9}cc/sec.

Plating of the copper-ceramic final assembly will be accomplished with gold rather than nickel for increased frequency performance.

Process Evaluations

Higher temperature and more reliable contact metallizing methods and materials have been under investigation and several merit intensive evaluation.

Methods of mounting wafers for scribing-for-dicing, which will eliminate the use of waxes, are still being developed.

In order to increase the reliability of the large area devices, new methods and materials used in dice mounting are being evaluated.

Cleaning and surface preparation methods, applied to mounted assemblies prior to capping, have been under intensive investigation; however, no superior method has thus far been discovered.

11/16 Coldweld Copper-Ceramic Package (Figure 2.4.1)

The general outline of this package is the same as the 11/16 nickel-iron resistance welded package previously used. The primary advantages of the copper-ceramic package lies within its use of copper for stud, stud pin, cap and cap tube material, and the use of ceramics as an insulation media. The copper-ceramic seal does not have the high frequency limitations experienced with a glass-nickel-iron compression seal. Power losses experienced with the glass-nickel-iron seals, as close as could be determined, were in the 5% to 15% range, while losses due to the copper-ceramic seals are apparently something less than 1% to 2%.

While accurate design of package and coldwelding dies is necessary to preclude base deformation in the coldweld operation, a highly reliable weld can be achieved without danger of weld splatter, which is an ever present control problem with resistance welding.

A modified version of this package will be employed in the assembly of the redesigned device. Since the design of the new package is 90% complete, the details will be presented in the next Quarterly Report.

Assembly Equipment

Some of the more notable acquisitions were:

A. A Kulicke and Soffa "Auto Probe" has been purchased to be used in conjunction with a Kulicke and Soffa Automatic Computer Type

Test Set, which will provide capabilities of measuring BV_{CES}, BV_{EBO} and h_{FE} at test limits greater than previously available.

B. The latest model thermocompression nailhead leadbonder has been purchased for this contract. Among its newest features are provisions for stitch bonding. With its greater versatility and more rapid bonds, methods, rates and yields heretofor difficult or impossible, can be achieved.

C. A large Dennison Press has been ordered for coldwelding operations.

D. A mounting station, scribing machine and other various assembly equipment has been procured.

Further purchases of assembly equipment will be made as the need requires.

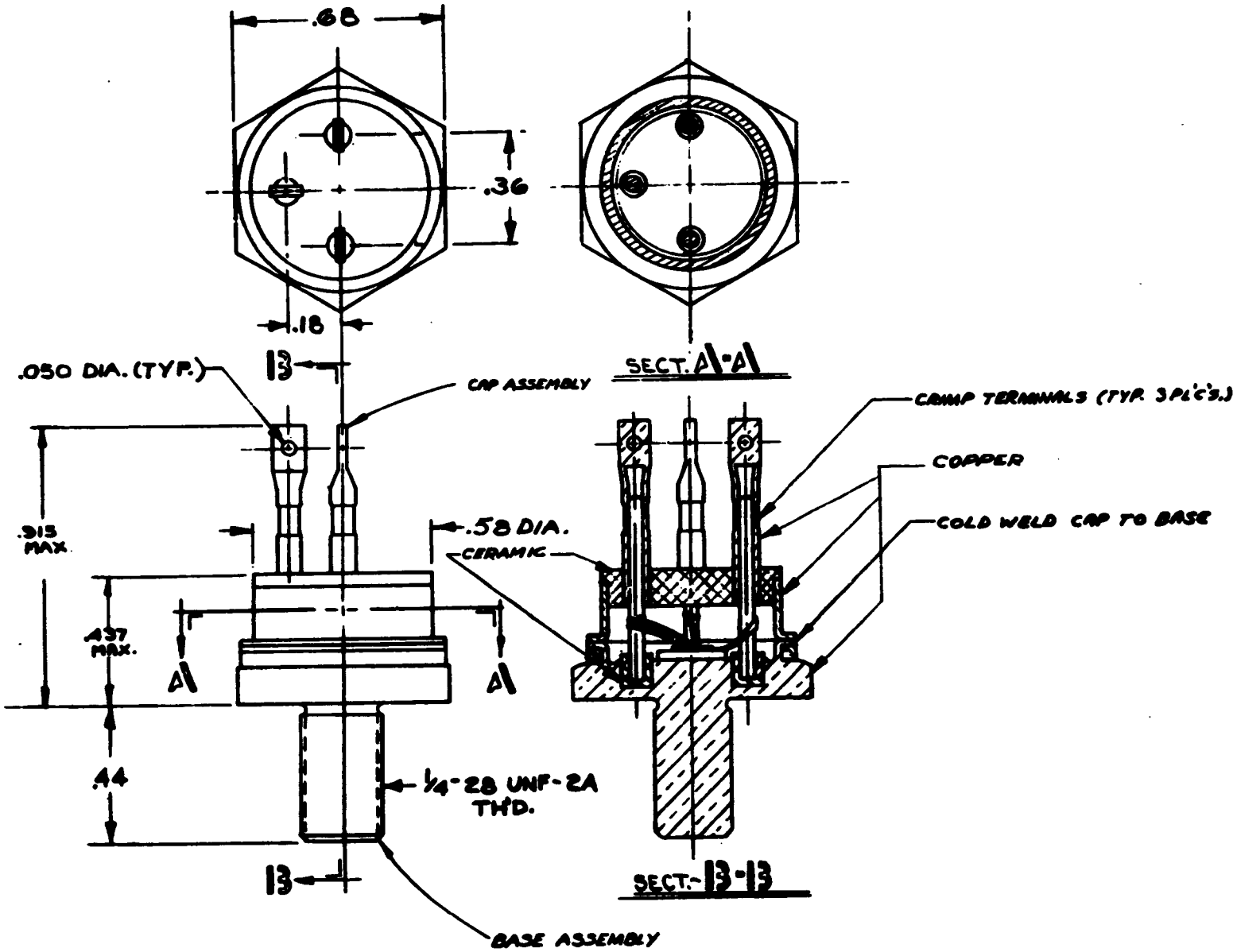

.68
.36
.18
13
.050 DIA. (TYP.)
CAP ASSEMBLY
SECT. A-A
CRIMP TERMINALS (TYP. 3 PL'C'S.)
COPPER
COLD WELD CAP TO BASE
.58 DIA.
CERAMIC
.315 MAX.
.437 MAX.
A
A
.44
1/4-28 UNF-2A TH'D.
13
SECT. 13-13
BASE ASSEMBLY

Figure 2.4.1

Chapter 3

Testing

3.1 Introduction

A review of the various electrical tests performed during the processing sequence is made, and the information obtainable therefrom is included in the following paragraph. More important is a set of curves, together with a verbal discussion of each curve, describing in more detail the performance of this transistor. Curves of h_{fe} versus current, voltage and frequency are given which show that the present device is indeed optimized around 600 ma and 80 volts at a bias point. Included also is another plot of the second breakdown locus. The locus confirms our findings reported in the Third Quarterly Report of this contract - DA 36-039 SC-86733 - as to the inability of the current device to handle the required power dissipation.

The use of the new design, outlined in Chapter 2, Paragraph 2.2, is designed to eliminate this problem.

3.2 Electrical Testing

All units in process are either spot checked or 100 percent tested for device performance while in wafer form, as dice, and as transistor assemblies (leadbonded or capped units) in accordance with the following test processing procedure:

A. Base Scope on Wafer

Tested after base diffusion and prior to emitter diffusion to check the V-I characteristics of the collector-to-base junction.

B. Emitter Scope on Wafer

After emitter has been diffused, a great deal of useful information, concerning control of all prior diffusion processes, can be generated by examining the DC pulsed common emitter current gain (h_{FE}) and V-I characteristics of both collector-to-base and emitter-to-base junctions.

C. Metallizing Scope

All wafers are spot checked, after metallizing, for the same critical parameters as stated above in Step B to make sure that contact metallizing has not degraded the basic characteristics of the device.

D. Dice Scope

All good wafers from Step C will be diced and inspected for visual rejects. Accepted dice are then screened for

electrical characteristics by employing the computer-driven sorting machine on basis of DC Beta and junction characteristics.

E. Leadbond Scope

After the dice are mounted and leadbonded, it is possible to test the device under conditions approximating the desired operating levels. At this stage, the sub-standard devices which fail to meet the following critical parameters are rejected:

1. Breakdown characteristics
2. Leakage at specified voltage
3. Power gain at operating frequency
4. Contact resistance
5. DC Beta at specified bias level
6. Opens and shorts

F. Final Electrical Test

Final Electrical Test is performed after capping and environmental sequence as per specifications as described in Appendix "B".

At the end of each stage of scope testing, the causes for rejects are thoroughly investigated.

Beyond processing the above tests, some of the standard units are subjected to an extensive series of tests to characterize this 25W-100MC transistor. Supplementing the technical information included in the Third Quarterly Report, the manufacturer has obtained additional data regarding its electrical characteristics.

Listed below is a set of typical characterization curves plotted from the average readings of a large group of units at specified conditions:

A. Frequency Dependence of h_{fe} in db (V_{CE}, I_C)

Figures 3.2.1, 3.2.2, and 3.2.3 display a set of typical curves for h_{fe} as a function of frequency at varying current and voltage bias levels. All measurements are taken with a Transfer Function Bridge built by General Radio Corporation.

The negative slope of h_{fe} within the frequency band from 40 to 400 MC (on log scale) changes at the rate of 2 to 5 decibels per octave as the collector current is increased from 50 to 300 MA at fixed voltage (5, 10 or 20V).

With collector-to-emitter voltage biased at 5 or 10 volts, h_{fe} begins to fall off somewhere between 300 and 600 MA collector current. This is why, at the same operating frequency, h_{fe} at I_C = 600 MA is lower than that at I_C = 300 MA (see Figures 3.2.1 and 3.2.2). At a constant collector

current of 50 or 100 MA, the effect of frequency on change of h_{fe} is more pronounced at higher voltage bias levels.

The approximate values for gain bandwidth product (f_T), alpha cutoff frequency ($f_{\alpha e}$) at the various voltage and current levels can be estimated or computed from these curves.

B. Second Breakdown Locus

Figure 3.2.4 is a drawing of typical second breakdown locus for the 75W-PEM device as currently designed and fabricated. The locus do not exhibit the constant power dissipation at the various bias levels, but display the typical shapes for this type of failure mechanism.

C. Power Gain as a Function of Current and Voltage

Power gain was measured at the following current and voltage levels on 10 units at the same operating frequency of 100 MC and the same power input of 2.5 watts, as used on standard units (measured at I_C = 600 MA, V_{CE} = 80V):

	V_{CE} (V)	I_C (MA)	Power Gain Watts	db.
	50	800	16	8
(control)	80	600	24	10
	100	400	16	8

This data reveals that the standard bias conditions for the power gain measurement is close to optimum at 50% collector efficiency.

D. h_{fe} (In Current Ratio) vs Frequency (On Log Scale) - (I_C, V_{CE})

The change of h_{fe} in current ratio due to frequency at the various bias level is plotted on the expanded scale (Figures 3.2.5, 3.2.6 and 3.2.7) to bring out every detail of the effect of operating frequency and bias level on small signal common emitter transfer ratio.

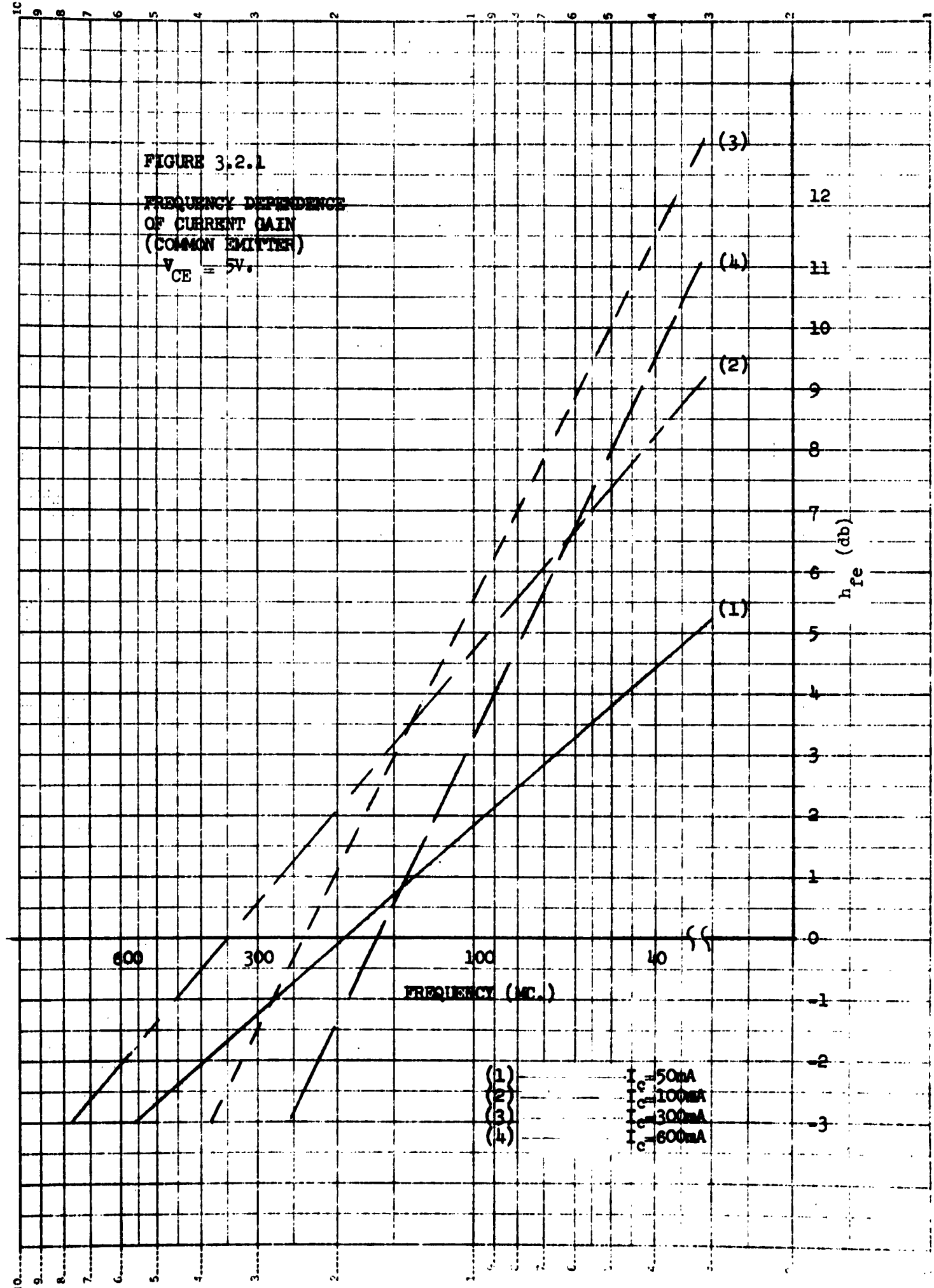
E. h_{FE} as a Function of V_{CE} or I_C

Variations of DC pulsed beta over a wide range of current at collector-to-emitter voltage from 1 to 20V and 25 to 70V (as plotted from average readings of two different groups of units) are shown in Figures 3.2.8 and 3.2.9, respectively. It appears that h_{FE} increases with collector current at a slightly faster rate at higher voltage. The lesser spread-out of beta between I_C = 30 and 50 MA, as shown in Figure 3.2.9, may not be of any significant value because the equipment error for h_{FE} measurement may overshadow such a small deviation.

The falloff of beta at approximately 200 MA is only noticeable when the voltage is biased at one volt (Figure 3.2.8). At all other voltage bias levels (up to 70V), some of h_{FE} values keep on increasing even after the current has reached 600 MA. If

this device is checked at voltage in excess of 70V, it will be driven into the second breakdown region before the current gain can be measured at some reasonably high current level.

Figure 3.2.10 displays the typical curves for h_{FE} as a function of collector-to-emitter voltage (V_{CE}) over a current range of 10 to 300 MA. The reader will note that, between 100 and 300 MA, the effect of current on the change of h_{FE} is more pronounced at higher voltage.



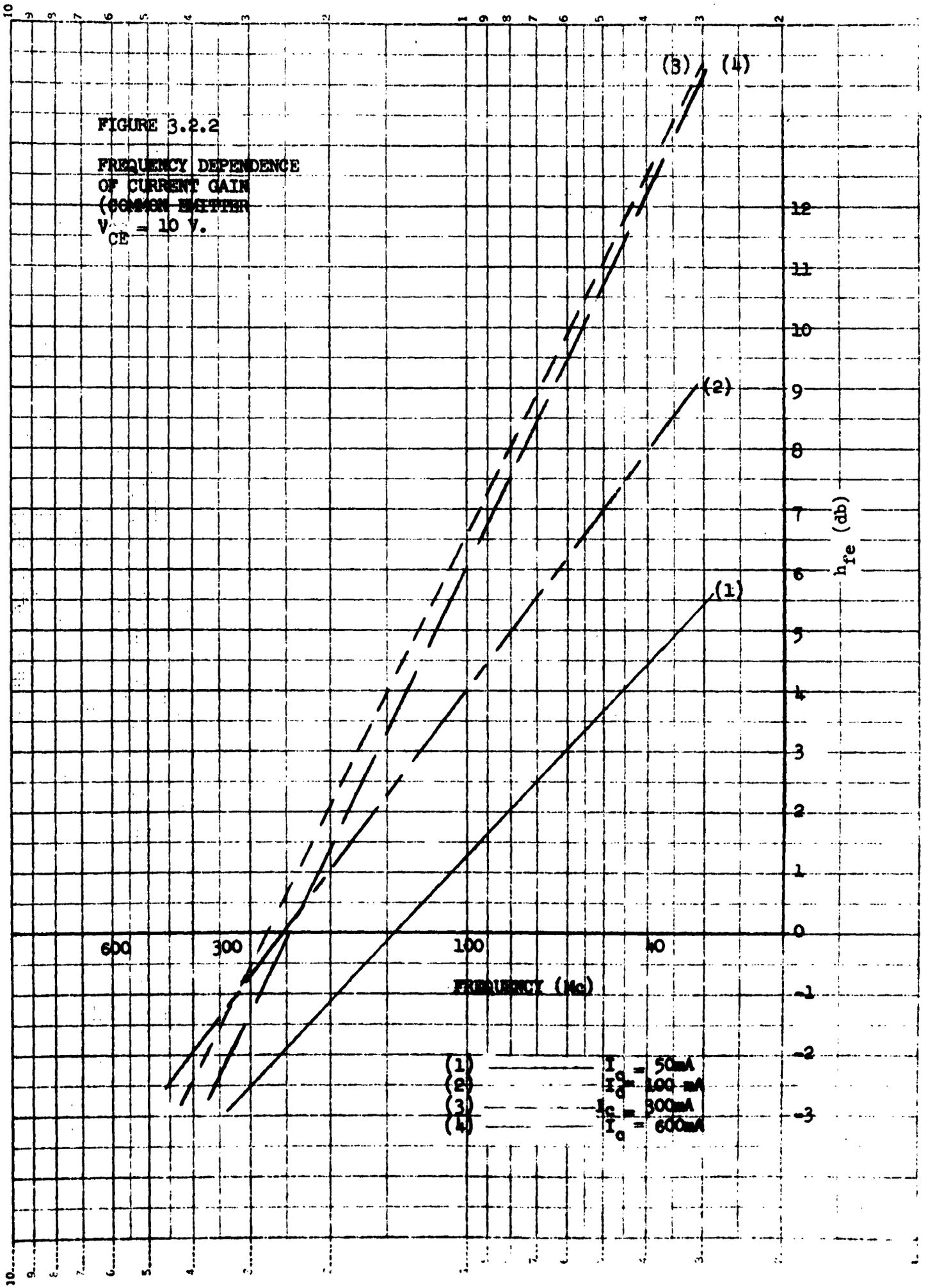
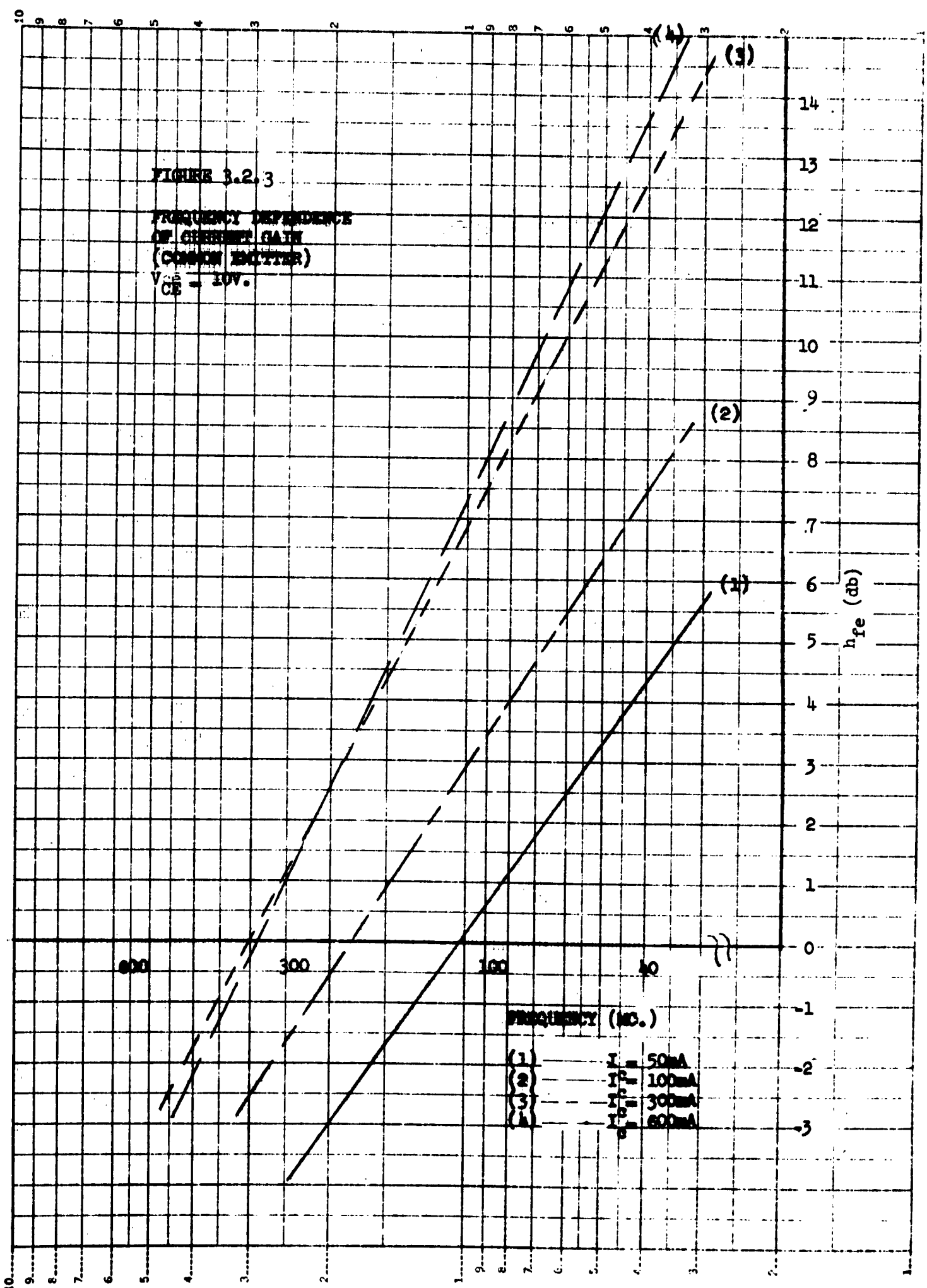
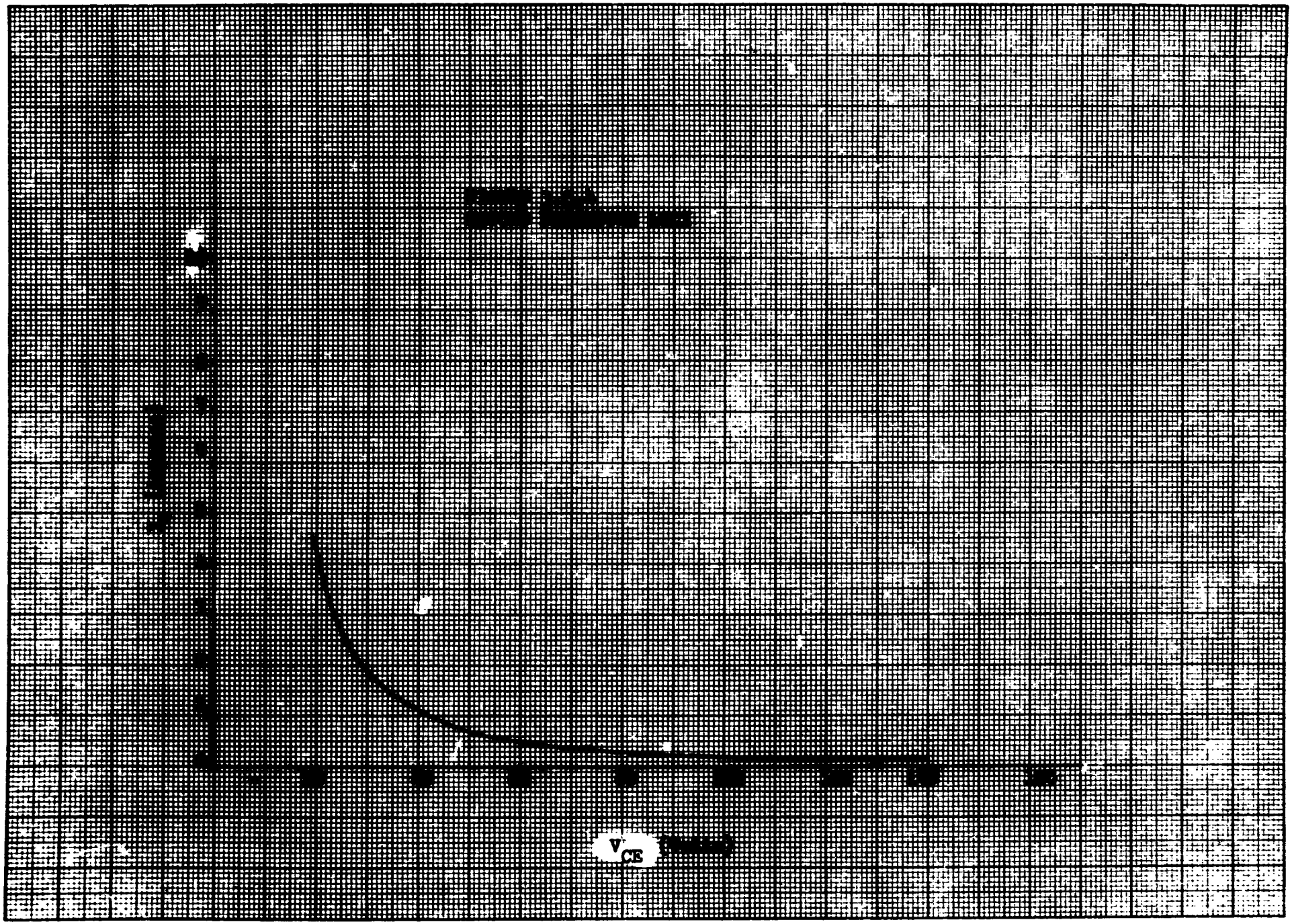


FIGURE 3.2.2
FREQUENCY DEPENDENCE OF CURRENT GAIN (COMMON EMITTER
V_{CE} = 10 V.
(1)
(2)
(3)
(4)
600
300
100
40
FREQUENCY (Mc)
h_{fe} (db)
12
11
10
9
8
7
6
5
4
3
2
1
0
-1
-2
-3
(1) I_C = 50mA
(2) I_C = 100 mA
(3) I_C = 300mA
(4) I_C = 600mA





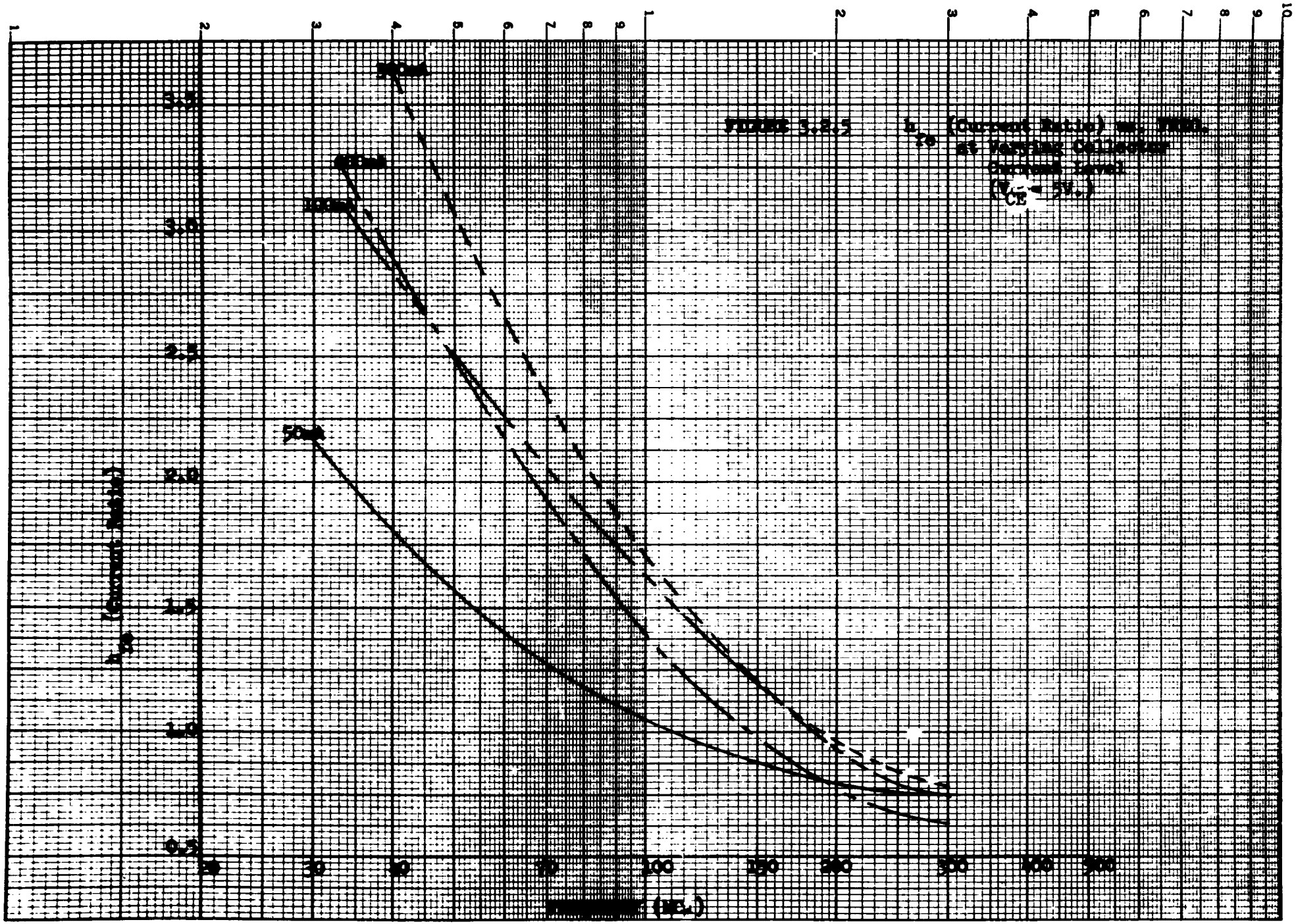


FIGURE 3.2.5 h_{fe} (Current Ratio) vs. I(mA), at Various Collector Current Level (V_{CE} = 5V.)

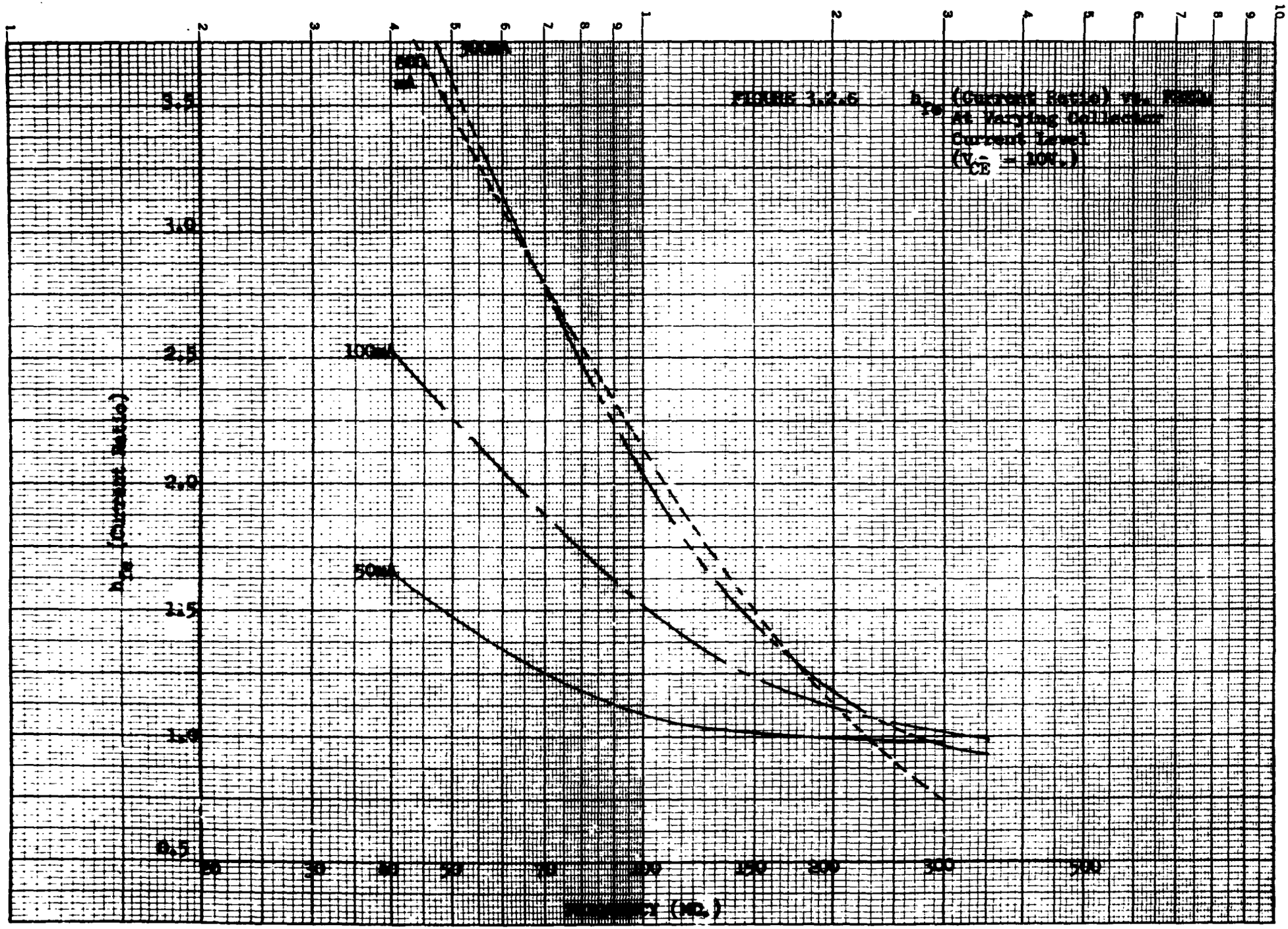


FIGURE 3.2.6 h_{fe} (Current Ratio) vs. Frequency At Varying Collector Current Level (V_{CE} = 10V.)

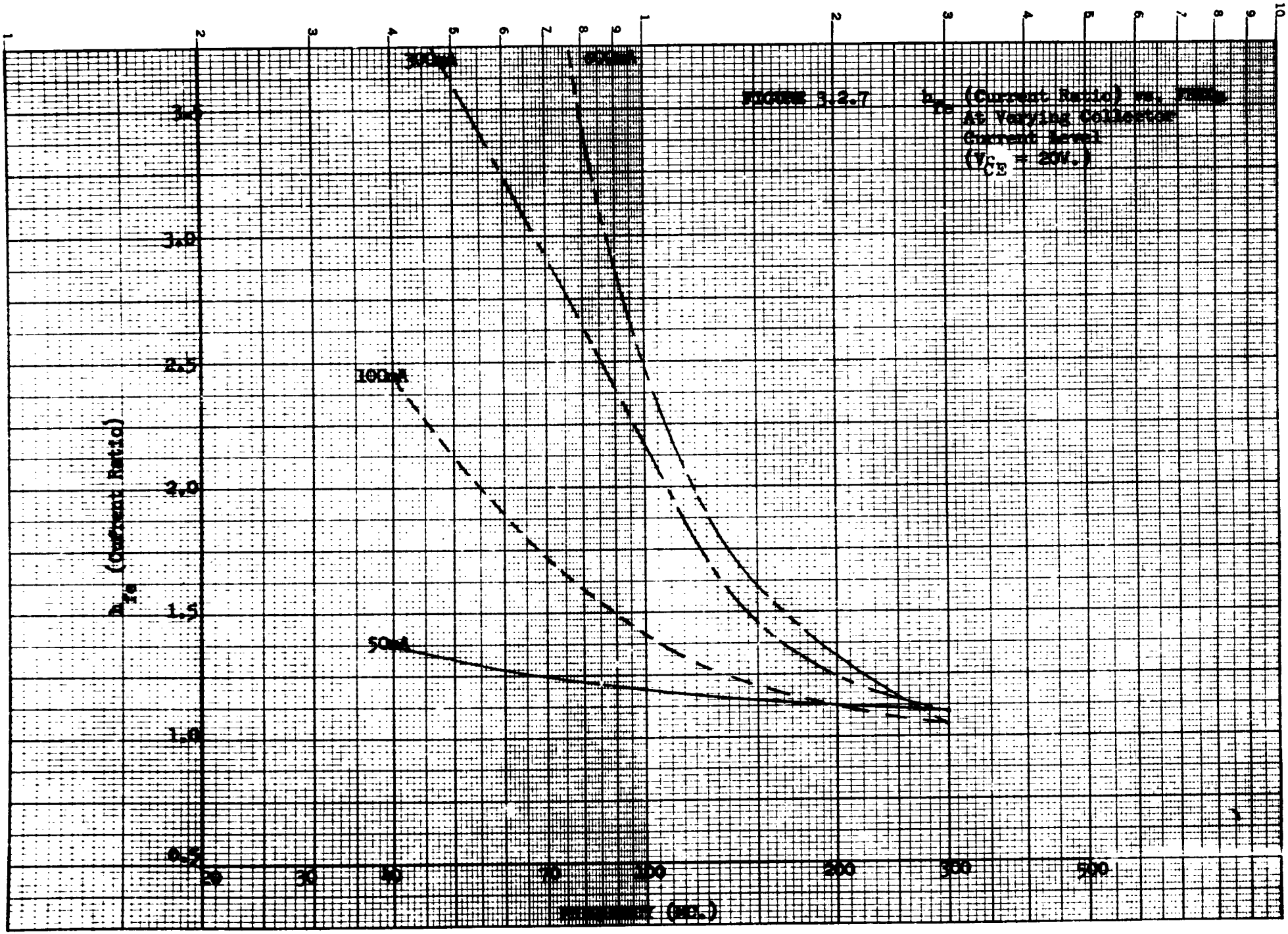
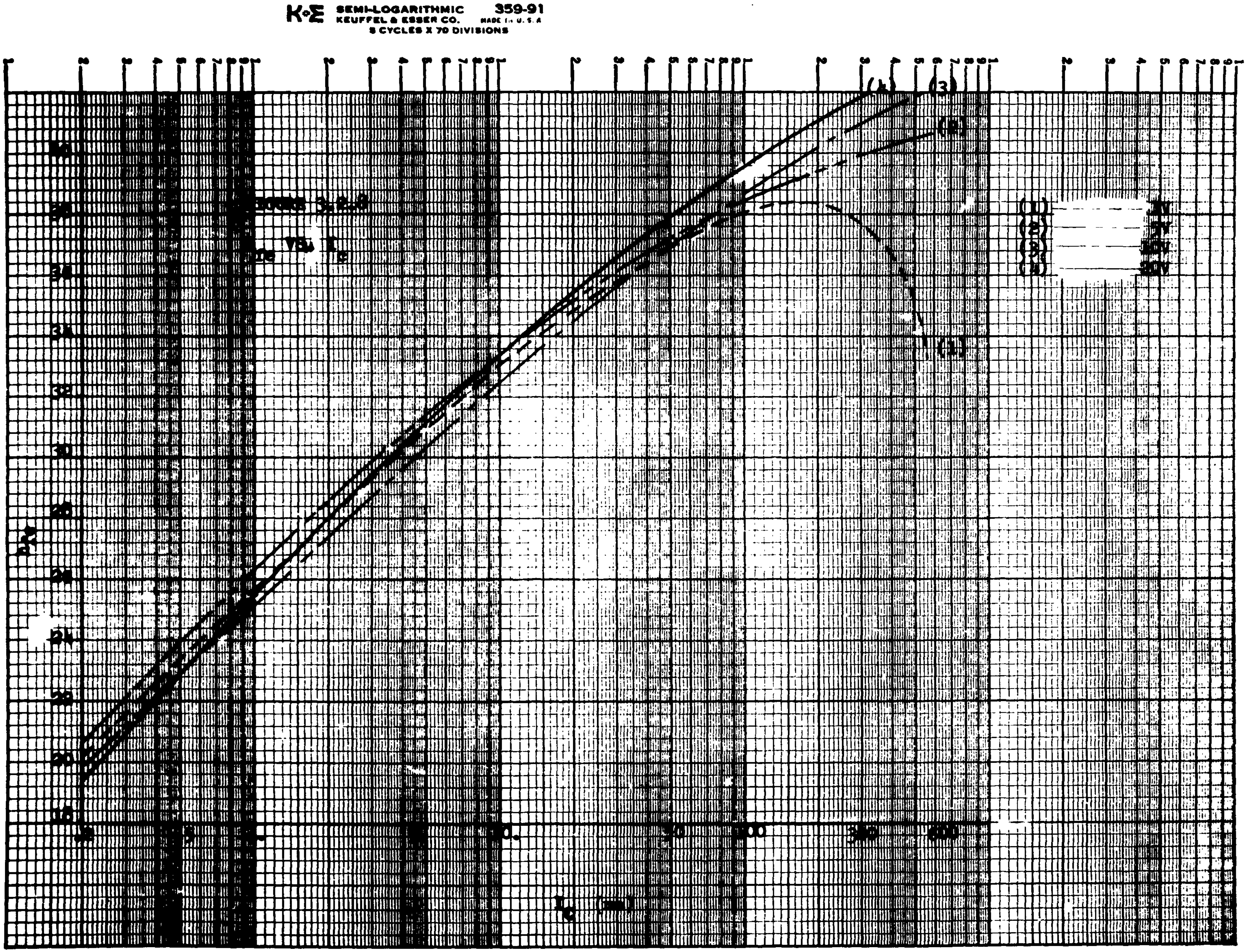


FIGURE 3.2.7 h_{fe} (Current Ratio) vs. Frequency At Varying Collector Current Level (V_{CE} = 20V.)



K&E SEMI-LOGARITHMIC 359-91
KEUFFEL & ESSER CO. MADE IN U.S.A.
5 CYCLES X 70 DIVISIONS
(1)
(2)
(3)
(4)
20
22
24
26
28
30
32
34
36
38
40
10.
100

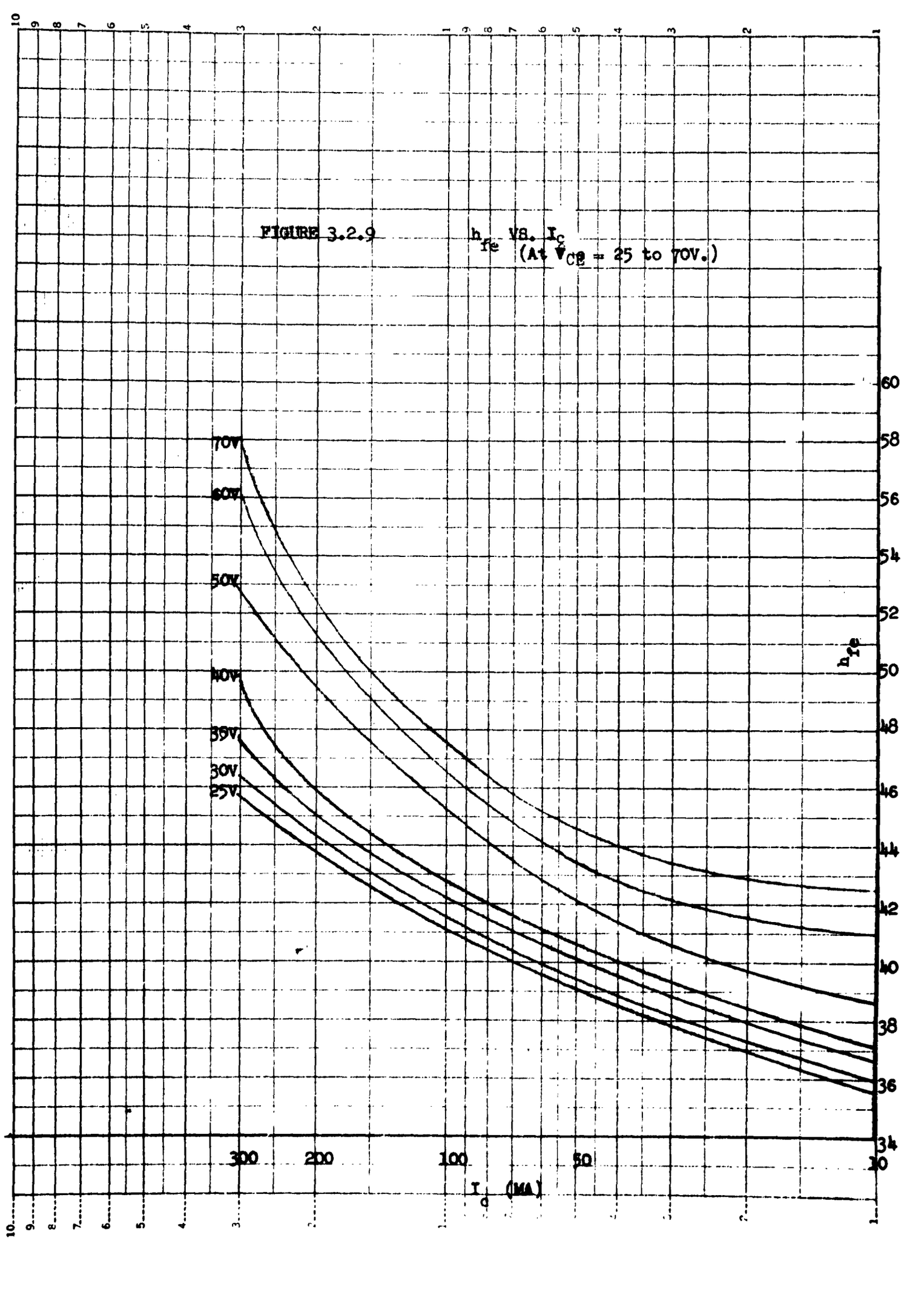
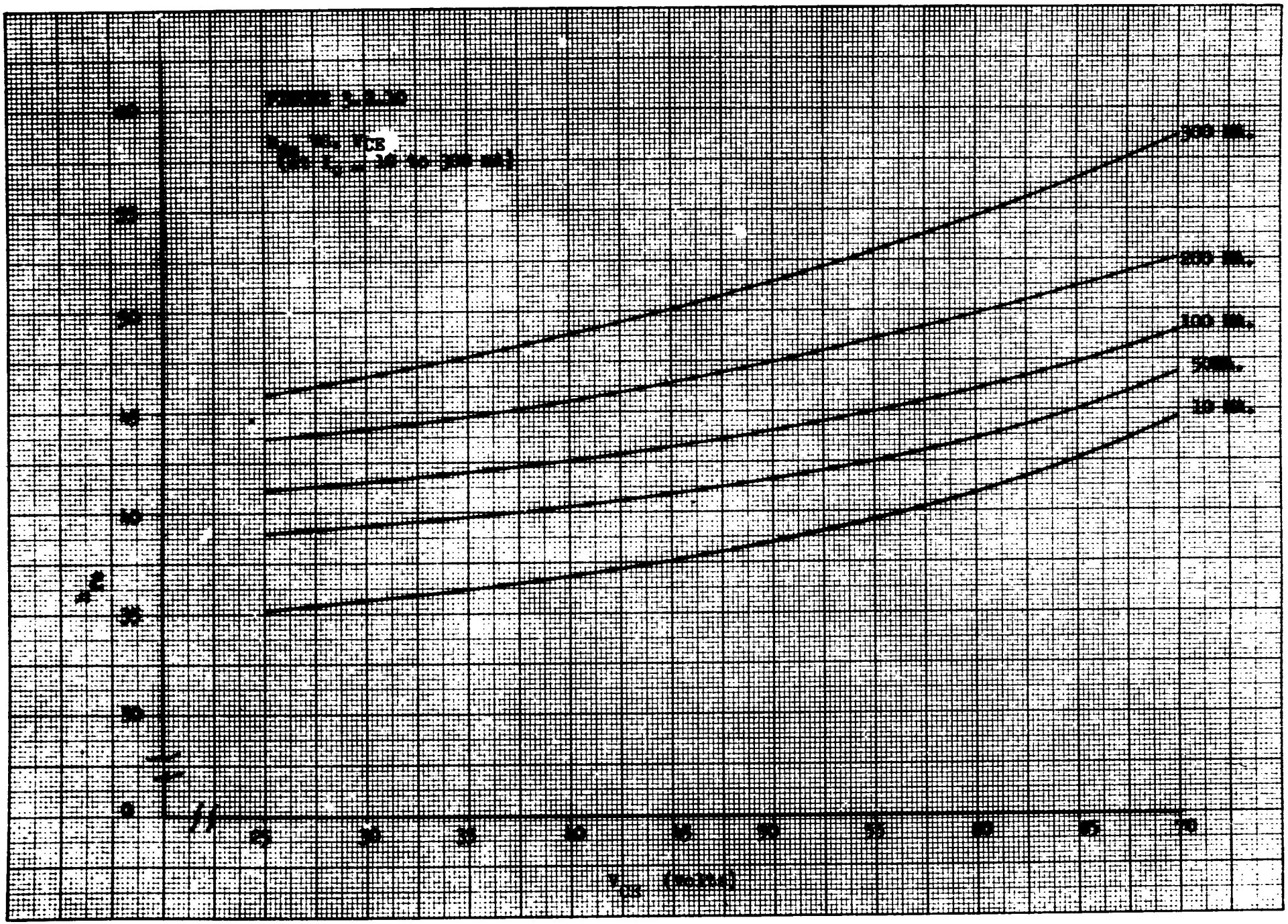


FIGURE 3.2.9
h_{fe} VS. I_C
(At V_{CE} = 25 to 70V.)
70V
60V
50V
40V
35V
30V
25V
h_{fe}
60
58
56
54
52
50
48
46
44
42
40
38
36
34
300
200
100
50
10
I_C (MA)



SECTION IV - SUMMARY AND CONCLUSION

This report has two essential points to make:

1. From the theoretical design, and from the review of electrical performance in Paragraph 3.2, it can be seen that the device, as presently constituted, cannot perform as required in the critical power dissipation regimen.

2. Looking at the Design Section, we find two possible alternate designs. The 70 volt bias level design involves a minimum of process changes and, because of its longer stripe length, provides better heat dissipation. However, the laws of physics dictate that problems will be encountered with the second breakdown failure mode. The use of this design can be made practical, but a large amount of effort on second breakdown prevention will be needed. The 80 volt design involves considerable reprogramming of processes and processing sequence. The net result of the high bias voltage design would increase susceptibility to the second breakdown failure mode. It is recommended that an additional look at a 25 volt - 2 ampere bias level design be undertaken.

SECTION V - PROGRAM FOR THE NEXT INTERVAL

The pilot line will be set up in its assigned location, new equipment; i.e., furnaces, lead bonders and hydraulic press installed and required operations begun to 'de-bug' the line.

The 70 volt devices will be fabricated and subjected to thorough tests.

The 25 volt design will be converted into physical form, i.e., engineering drawings and photo resist artwork, photo resist masks prepared and device construction commenced.

The modification of the copper-ceramic package will be completed.

Diffusion research will be continued, particularly in the field of oxidations.

SECTION VI - PUBLICATIONS, REPORTS AND CONFERENCES

There were no publications or conferences applicable to the contract during this quarter.

The Monthly Reports were:

The tenth Monthly Letter Report - submitted 9 May 1963

The eleventh Monthly Letter Report - submitted 14 June 1963

The twelfth Monthly Letter Report - submitted 12 July 1963

SECTION VII - IDENTIFICATION OF PERSONNEL AND EXPENDITURES

The following professionals have expended effort on the contract during the periods of interest; however, their biographies have not appeared heretofore.

Joan M. Crishal

Miss Crishal attended the University of Michigan where she received the B.S. degree in Chemical Engineering in 1948 and the M.S. degree in Chemistry in 1950.

From 1950-52 she was employed by the Public Health Service as a spectrographer. For the next two years she was in the U.S. Navy as a Lieutenant Junior Grade in communications. Miss Crishal joined PSI in September 1954. Her initial assignments were in the areas of semiconductor crystal growth, etching, evaporating, plating, and lifetime measurement. She also engaged in studies of surface treatments for control of device characteristics. This work led to her development of new diffusion processes for the planar structure. Miss Crishal is now actively at work on diffusion process control and leakage problems of large area transistors.

William C. Newell

Mr. Newell received a B.S. degree in Engineering Physics from the University of Washington, a M.S. in Physics from U.C.L.A.

He has had two years experience in the semiconductor field prior to joining Pacific Semiconductors, Inc.

While at Solid State Radiations, his primary effort was in the evaluation of developmental detector devices. His later efforts were directed toward a research program conducted for the purpose of determining neutron and gamma radiation damage effects on silicon detectors.

Mr. Newell joined Pacific Semiconductors in June 1962 and has since been working on the development of production processes for the manufacture of high power transistors.

Kenneth O. Tillung

Mr. Tillung received the B.S. degree in Aeronautical Engineering from the University of Chicago in 1952.

He served in the U.S. Navy for two years as a Communications and Electronics Officer aboard a destroyer. From late 1954 to mid 1956 Mr. Tillung was employed by Gardner Machine Company as a Design Engineer specializing on heavy grinding equipment. From August of 1956 to November of 1958 he was a project engineer at the Warner Electric Brake and Clutch Company.

Mr. Tillung joined Pacific Semiconductors, Inc., in November of 1958 and was originally concerned with the design and development of automatic multi-stage equipment for semiconductor device manufacturing. He progressed to projects involving process and packaging development and has specialized in high-power and high-frequency transistor development for the last two years.

Mr. Tillung is a member of the American Society of Mechanical Engineers.

Man Hour Labor Expenditures

Effort expended by professional employees:

Name	Hours
Chao, P. Y.	16
Crishal, J. M.	12
Lamoureux, R. T.	392
Neville, R. C.	206
Newell, W. C.	40
Podell, J. F.	344
Preletz, M. O.	130
Tillung, K. O.	72
Treleaven, D. H.	120
	1,332
Technical:	3,239
TOTAL:	4,571

APPENDIXES

APPENDIX A

SIGNAL CORPS TECHNICAL REQUIREMENTS

TRANSISTOR, SILICON, VHF, POWER (75 WATT) TYPE SigC-2N(X-6)

1. SCOPE

1.1 Scope. - This document covers the detail requirements for silicon, VHF, Power Transistors capable of delivering 25 watts of output power with 10 db of power gain at 100 mc.

1.2 Maximum ratings at 25°C. (See 3.2 herein):

BV_{CBO}	BV_{CES}	BV_{EBO}	I_C	P_C	T_J	T_{stg}
Vdc	Vdc	Vdc	Adc	W	°C	°C
180	180	5	1.5	75 (at: T_C= 25°C)	200	-65 to + 200

2. APPLICABLE DOCUMENTS

2.1 The following documents, of the issue in effect on date of invitation for bias, form a part of this specification to the extent specified herein:

SPECIFICATIONS

MILITARY

MIL-F-14072	Finishes For Ground Signal Equipment
MIL-S-19500	Semiconductor Devices, General Specification For

STANDARDS

MILITARY

MIL-STD-202	Test Methods For Electronic and Electrical Component Parts

DRAWINGS

SIGNAL CORPS

SC-A-46600 — Preproduction Sample Approval in Lieu of Requirements in Specifications.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring agency or as directed by the contracting officer. Both the title and number or symbol should be stipulated when requesting copies.)

3. REQUIREMENTS

3.1 Requirements.- Requirements for the transistors shall be in accordance with Specification MIL-S-19500 and as specified herein.

3.2 Abbreviations and symbols.- The abbreviations and symbols used herein are defined in Specification MIL-S-19500 and as follows:

P_i . . . . . power input

P_o . . . . . .power output

LV_{CES} . . . . . sustaining voltage (collector-to-emitter) base short-circuited

3.3 Design and construction.- The design and construction of the transistors shall be in accordance with applicable requirements of Specification MIL-S-19500.

3.3.1 Transistor case.- The transistor case shall incorporate a stud with a mounting nut and lock washer, physically located at the end of the case opposite the leads, to enable ready mounting of the transistor and dissipating the required power. The transistor case shall be electrically insulated from the collector, emitter, and base.

3.3.2 Operating position. - The transistors shall be capable of proper operation in any position.

3.3.3 Finishing of external metallic surfaces.- The finishing of external metallic surfaces shall be in accordance with requirements in Specification MIL-F-14072 for surface classification Type II, except that the requirements in Specification MIL-F-14072, Section 3, Requirements, covering moisture resistance and finish resistance, and Section 4, Quality Assurance Provisions therein, shall not be applicable. If, due to

special conditions of service or design, a contractor desires to use finishes, materials, or processes other than those specified, such proposal including the reasons therefore shall be submitted to the Contracting Officer for approval. At the discretion of the Contracting Officer, samples and test data may be required to substantiate the suitability of the proposed substitute(s).

3.4 Performance characteristics.- The transistor performance characteristics shall be as specified in Tables I and II herein. (See 6.3 herein.)

3.5 Marking.- The transistors shall be marked in accordance with Specification MIL-S-19500 and as follows. In instances where the diminutive size or lack of suitable surface area on the device would prevent a marking accomplishment readable by the unaided eye, 20/20 vision, at eight inches distance from the device, such marking may be omitted directly on the device. All required marking shall be placed on the unit package.

3.5.1 Type-designation marking.- The transistors shall be marked with the letters "SigC" and the "2N" designation of the device. The "2N" designation of the device shall be "(X-6)" until an identification number conforming to the type designation requirements of Specification MIL-S-19500 has been established.

4. QUALITY ASSURANCE PROVISIONS

4.1 General. - Except as otherwise specified herein, the responsibility for inspection, general procedures for acceptance, classification of inspection, and inspection conditions and methods of test shall be in accordance with Specification MIL-S-19500, Quality Assurance Provisions.

4.2 Preproduction Sample Approval. - The Preproduction Sample approval requirements in Signal Corps Drawing SC-A-46600 hereby replace any Qualification requirements referable to the product covered herein.

4.3 Sampling and acceptance criteria for Acceptance Inspection (see 6.2 herein).- For all tests except Life tests, sampling and acceptance criteria shall be in accordance with 4.3.1 and 4.3.2, respectively, herein for Life tests, sampling and acceptance criteria shall be in accordance with requirements for Method B in Specification MIL-S-19500, Appendix C. The respective LTPD (Lot Tolerance Percent Defective) and Max. Acc. No. (Maximum Acceptance Number) requirements in Tables I and II herein shall govern relative to the details in 4.3.1 and 4.3.2 herein.

4.3.1 Sample Size. - The sample size shall be selected by the manufacturer using Table III herein. The sample size so chosen shall be within the Max. Acc. No. limit associated with the LTPD specified in Tables I and II herein.

4.3.2 Sample acceptance criteria.- For the sample size tested, the Acceptance Number "(a)" in Table III shall not be exceeded. (Rejection number "r" = "(a)" + 1.)

4.4.4 Tightened inspection.- Tightened inspection on resubmitted lots is obtained by testing to an LTPD equal to or less than one-half of the specified initial LTPD.

4.4 Specified LTPD and Max. Acc. No.- The LTPD and Max. Acc. No. specified for a subgroup in Tables I and II herein shall apply for all of the tests, combined, in the subgroup.

4.5 Destructive tests.- The Group B, Subgroups 2, 3, 4, 5, 6, and 7 tests are considered destructive. However, the tests of Subgroups 2, 3, 4, 5, 6, and 7 can be considered non-destructive if sufficient evidence is presented to the Government inspection authority to that effect. Acceptable evidence, for example, would be repeating of all Subgroups 2, 3, 4, 5, 6, and 7 tests, ten times, without significant device degradation. This test repetition procedure need be done only once at inception of Acceptance Inspection, provided that no change in design, or of production techniques, has been effected.

4.6 Disposition of sample units.- Sample units that have been subjected to and have passed Group B, Subgroups 2, 3, 4, 5, 6 and 7 tests not determined to be destructive tests may be delivered on the contract sample units are subjected to and pass Group A inspection. Defective units from any sample group that may have passed group inspection shall not be delivered on the contract or order until the defect(s) has been remedied to the satisfaction of the Government.

4.7 Particular examination and test procedures.-

4.7.1 Sustaining Voltage Test. - The sustaining voltage of the collector with respect to the emitter shall be measured under the conditions specified, with the base short-circuited to the emitter.

4.7.2 Oscillator Power Output Test.- The specified voltage and current shall be applied to the respective terminals under the conditions specified and the power output of the oscillator shall be measured at the frequency specified.

4.7.3 Base Spreading Resistance test.- The specified voltage and current shall be applied to the respective terminals, with the transistor in the common-emitter configuration. An a-c small signal of the high frequency specified shall be applied to the input terminals, and the output terminals shall be short-circuited. The real part of the short-circuit input impedance shall be measured and assumed equal to the base spreading resistance.

4.7.4 Tension test.- The specified force shall be applied to each

lead in the direction of the axis of the lead. The force shall not be applied to more than one lead at a time, and all leads shall be tested.

4.7.5 Torque Test.- The specified torque shall be applied to the stud and about its axis. The stud shall not have become loosened nor the threads damaged, as a result of this test.

4.7.6 Bending Moment test - The transistor shall be mounted by the normal mounting means. The specified force shall be applied, without shock, at right angles to the lead and near the end of the lead.

Table 1. Group A Inspection

MIL-S-19500 Appendix C Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup I		Major:5 Minor:10	3 4				
30.13	Visual and mechanical Examination	---			---	---	---	---
	Subgroup II		5	3				
50.6	Collector cutoff current	V_{CB} = 180Vdc I_E = 0			I_{CBO}	---	5	mAdc
50.6	Emitter cutoff current	V_{EB} = 5 Vdc I_C = 0			I_{EBO}	---	5	mAdc
50.9	Collector cutoOf current	V_{CE} = 180Vdc V_{EB} = 0			I_{CES}	---	5	mAdc
50.9	Collector cutoff current	V_{CE} = 70Vdc V_{EB} = 0			I_{CES}	---	1	mAdc
50.40	Static forward-current Transfer ratio	V_{CE} = 50Vdc I_C = 1.5Adc			h_{FE}	10	---	---
50.40	Static forward-current Transfer ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	15	45	---
1/	Sustaining Voltage	I_C = 100mAdc V_{EB} = 0			LV_{CES}	90	---	Vdc
50.25	Saturation Voltage	I_C = 1.5Adc I_B = 300mAdc			$V_{CE(SAT)}$	---	0.75	Vdc

Table 1. Group A Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 3		5	3				
50.15	Power Gain	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc P_i = 2.5W $T_c \leq 55^{\circ}C$ 2/			P_g	10	---	db
3/	Oscillator power output	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc $T_C \leq 55^{\circ}C$			P_o	25	---	W
4/	Base Spreading Resistance	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc			r'_b	---	10	ohms
50.19	Output Capacitance	V_{CB} = 70Vdc I_E = 0 f = 1mc			C_{ob}	---	25	μμf
50.33	Small-signal short-circuit forward-current transfer ratio	V_{CE} = 70Vdc I_C = 715mAdc f = 100mc			h_{fe}	7	---	db

1/ See 4.7.1 herein.
2/ Test Circuit as mutually acceptable to Contracting Officer's Technical Representative and contractor.
3/ See 4.7.2 herein. Test circuit as mutually acceptable to Contracting Officer's Technical Representative and contractor
4/ See 4.7.3 herein.

Table II. Group B Inspection

MIL-S-19500 Appx. C Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup I		10	2				
30.9	Physical dimensions	---						
	Subgroup II		10	3				
40.12	Solderability	---			---	---	---	---
40.14	Temperature Cycling	$T_{(high)}$ = +200°C Test Cond. C 1/			---	---	---	---
40.16	Thermal Shock	$T_{(high)} = 100° \pm 3°C$ $T_{(low)} = 0° \pm 2°C$			---	---	---	---
40.6	Moisture Resistance	No initial conditioning			---	---	---	---
	End-point tests:							
30.9	Collector cutoff current	V_{CE} = 180Vdc V_{EB} = 0			I_{CES}	---	10	mAdc
30.9	Collector cutoff current	V_{CE} = 70Vdc V_{EB} = 0			I_{CES}	---	2	mAdc
30.6	Emitter cutoff current	V_{EB} = 5Vdc I_C = 0			I_{EBO}	---	10	mAdc
30.40	Static forward-current Transfer Ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	13	50	---

Table II Group B Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 3		10	3				
40.10	Shock	Non-operating 5 blows each in each orientation X1, Y1, Y2, Z1 (Total= 20 blows)			---	---	---	---
40.4	Constant acceleration (Centrifuge)	G = 20,000			---	---	---	---
40.18	Vibration, fatigue	V_{CB} = 20Vdc V_{EB} = 5Vdc			---	---	---	---
40.20	Vibration, variable frequency	---			---	---	---	---
	End-point Tests: Same as for Subgroup 2, above							
	Subgroup 4		10	3				
40.1	Barometric pressure (reduced)	Test Cond. B V_C-to-case = 180Vdc V_E-to-case = 180Vdc V_B-to-case = 180Vdc			---	---	---	---
30.6	High-temperature operation	T_A = + 150°C						
30.6	Collector cutoff current	V_{CB} = 70Vdc I_E = 0			I_{CBO}	---	10	mAdc

Table II. Group B Inspection - (continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Unit
	Subgroup 4 - Cont'd)							
30.7	Low-temperature operation:	T_A = -55°C						
50.40	Static Forward-Current Transfer Ratio	V_{CE} = 70Vdc I_C = 715mAdc			h_{FE}	8	---	---
30.11	Thermal resistance	---			θ_{J-C}	---	2.33	°C/W
40.9	Salt spray (corrosion)	Test Cond. A			---	---	---	---
	End-point tests: Same as for Subgroup 2, Above							
	Subgroup 5		10	3				
40.15	Tension	Force = 5 lb. 2/			----	----	---	---
40.17	Torque	Torque = 30 in/lb. 3/			---	---	---	---
4/	Bending moment	Force = 1 lb.			---	---	---	---
	Subgroup 6		λ 5	3	---	---	---	---
40.7	Storage Life	Method B $T_{Stg.}$ = +200°C			---	---	---	---
	End-point tests: Same as for Subgroup 2, above							

Table II. Group B Inspection - (Continued)

MIL-S-19500 Appx. C. Ref. Par.	Examination or Test	Conditions	LTPD	Max. Acc. No.	Symbol	Limits Min.	Limits Max.	Units
	Subgroup 7		$\lambda = 5$	3				
40.7	Operation Life	Method B V_{CB} = 20Vdc I_C = 350mA			---	---	---	---
	End-point Tests							
	Same as for Subgroup 2, Above							

1/ + Per Method 1032A in Standard MIL-STD-202.

2/ See 4.7.4 herein

3/ See 4.7.5 herein

4/ See 4.7.6 herein.

5. PREPARATION FOR DELIVERY

5.1 Preparation for delivery. - Preparation for delivery shall be in accordance with Specification MIL-S-19500.

6. NOTES

6.1 Notes. - The notes included in Specification MIL-S-19500, except for those covering qualification (see 4.2 herein) and the following, are applicable to this document.

6.2 Ordering data. - If this document is used with the "C" or later issue of Specification MIL-S-19500 containing LTPD-method Acceptance Inspection requirements, the solicitation should indicate that the Acceptance Inspection LTPD-methods requirements in paragraphs 4.3 through 4.3.3 herein shall be considered superseded by the pertinent requirements in the "C" or later issue of Specification MIL-S-19500.

6.3 Establishment of Additional Tests and Parameters.- The resolution of any additional tests and parameters that will serve for optimum performance evaluation of the device relative to the application need is encouraged. It is expected that such determination(s) will be by mutual agreement between the contractor and the responsible Government agency, and will be included in the final acceptance criteria, for the device. Pertinent electrical, physical, mechanical, and environmental test coverage in Specification MIL-S-19500 should be considered as a primary guide in this regard.

NOTICE: When Government drawings, specifications or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor any obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings, specifications, or other data isnnot to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any right or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

APPENDIX B

TEST DATA

APPENDIX B

This appendix presents the test data collected by Pacific Semiconductors, Inc., from the 75 devices that comprised the third "state-of-the-art" samples shipment made under Production Engineering Contract No. DA 36-039 SC-86733.

PACIFIC SEMICONDUCTORS, INC,
RESEARCH AND DEVELOPMENT DEPARTMENT
TRANSISTOR 254-100MC - TSM
[redacted]

Box No. 19

DATE 4-1-63
OPERATOR AB and HF
PAGE 1 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CE} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o (OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION					POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W V_{CE} = 80V f = 100 Mc I_C = 600mA		
												θ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	P_o	P_G	N
		V	V	µA	V	ratio	pf	V	f	W	%	°C/W	V	V	µA	ratio	W	db	%
	745	170	170	56.0	5.4	11.0	24.2	.30	8.5	24.4	50.8						25.8	10.14	53.8
	787	170	170	2.9	5.7	51.0	21.0	.20	8.5	24.4	50.8						25.1	10.02	53.2
	880	170	170	18.0	5.5	40.0	25.0	.10	9.0	25.6	53.4						25.2	10.03	52.5
	888	170	170	7.5	5.6	160.	24.7	.20	9.5	23.5	49.0						25.0	10.00	52.1
	964	170	170	45.0	5.8	>300	29.5	.05	7.5	23.1	48.0						23.0	9.63	48.0
	972	170	170	17.5	5.6	>300	25.2	.10	8.5	23.0	48.0						24.4	8.89	50.8
	1020	170	170	.170	5.6	30.0	23.9	.25	6.0	24.4	50.8						24.4	9.89	50.8
	1025	178	178	17.8	5.5	47.0	23.0	.20	5.7	26.2	54.6						25.0	10.00	52.1
	1036	172	172	.25	5.9	>300	24.2	.15	7.5	24.6	51.2						25.6	10.10	53.4
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.75 max	10 max	25 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

[redacted] SEMICONDUCTORS, INC,
[redacted] AND DEVELOPMENT DEPARTMENT
[redacted] 254-100MC - TEM
[redacted]

Box No. 20

DATE 5-8-63
OPERATOR AB and HF
PAGE 2 OF 9

[redacted] NO.	TEST NO.	V_{CBO} @ I_C = 100 mA	V_{CER} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CE} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o(OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION					POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W V_{CE} = 80V f = 100 Mc I_C = 600mA		
												θ J-C	V_{C30} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} =80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	P_o	P_G	η
		V	V	µA	V	ratio	pf	V	Ω	W	%	°C/W	V	V	µA	ratio	W	db	%
	1039	170	170	24.5	5.8	>300	21.8	.20	8.0	23.5	49.0						24.5	9.91	51.0
	1041	174	174	109.	5.5	56.0	20.8	.25	6.7	28.0	58.4						27.0	10.33	56.3
	1042	178	178	16.0	5.5	58.0	20.9	.40	6.5	28.0	58.4						25.4	10.07	52.9
	1043	170	170	17.4	5.3	23.0	23.1	.22	5.0	25.0	52.1						23.5	9.73	49.0
	1044	178	178	22.6	5.3	14.0	22.2	.98	4.7	26.7	55.6						24.4	9.89	50.8
	1045	176	176	86.0	5.3	14.0	23.2	.95	4.0	26.7	55.6						24.0	9.82	50.0
	1046	168	168	.0018	5.3	27.0	24.3	.15	5.7	25.4	52.9						25.2	10.03	52.5
	1047	170	170	54.0	5.2	13.5	23.0	.89	5.0	26.4	55.0						24.2	9.85	50.4
	1048	172	172	195.	5.6	225.	21.2	.12	6.7	27.5	57.3						26.6	10.27	55.4
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.75 max	10 max	25 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

PACIFIC SEMICONDUCTORS, INC,
RESEARCH AND DEVELOPMENT DEPARTMENT
TRANSISTOR 254-100MC - TYPE [redacted]

Box No. 21

DATE 5-31-63
OPERATOR AB and HF
PAGE 3 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CE} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o(OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION						POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W V_{CE} = 80V f = 100 Mc I_C = 600mA		
												θ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	P_o	P_G	N
		V	V	μA	V	ratio	pf	V	Ω	W	%	°C/W	V	V	μA	ratio	W	db	%
	1052	170	170	10.7	5.4	30.0	24.0	.20	6.0	25.0	52.1						23.6	9.74	49.2
	1054	184	184	3.8	5.3	13.0	22.5	.70	5.0	28.6	59.6						26.5	10.25	55.2
	1056	184	184	.49	5.3	15.0	22.0	.50	5.2	26.2	54.6						25.0	10.00	52.1
	1057	173	173	16.0	5.3	20.0	24.8	.30	5.5	24.6	51.2						23.0	9.63	48.0
	1058	170	170	.025	5.4	22.0	23.0	.30	4.0	25.6	53.4						25.6	10.10	53.4
	1059	172	172	.0008	5.6	34.0	22.5	.20	5.2	25.2	52.5						23.7	9.76	49.4
	1061	171	171	187.0	5.3	16.0	23.0	.40	4.0	26.2	54.6						26.0	10.17	54.2
	1051	184	184	6.40	5.3	13.0	23.0	1.30	4.2	26.0	54.2						25.0	10.00	52.1
	1076	182	182	110.	5.3	24.0	50.0	.70	7.0	28.6	59.6						26.0	10.17	54.2
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.75 max	10 max	25 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

PACIFIC SEMICONDUCTORS, INC,

RESEARCH AND DEVELOPMENT DEPARTMENT

TRANSISTOR 25W-100MC - TYPE [redacted]

Box No. 22

DATE 6-4-63

OPERATOR AB and HF

PAGE 4 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CE} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o (OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION					POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W V_{CE} = 30V f = 100 Mc I_C = 600mA		
												θ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	P_o	P_G	N
		V	V	µA	V	ratio	pf	V	°	W	%	°C/W	V	V	µA	ratio	W	db	%
	1077	176	176	67.0	5.5	19.0	24.0	.30	7.0	29.4	61.3						28.2	10.52	58.8
	1078	190	190	95.0	5.4	49.0	22.3	.30	8.5	30.2	63.0						27.0	10.33	56.3
	1079	176	176	89.0	5.4	40.0	23.0	.30	7.5	28.3	59.0						27.3	10.38	56.9
	1080	178	178	8.7	5.5	45.0	22.6	.40	7.0	28.2	58.8						26.6	10.27	55.4
	1081	181	181	180.	5.4	18.0	26.8	.40	6.7	26.7	55.6						25.0	10.00	52.1
	1082	184	184	16.2	5.4	30.0	22.5	.50	7.5	28.2	58.8						25.0	10.00	52.1
	1083	181	181	38.4	5.5	20.0	22.2	.75	7.5	28.0	58.4						25.7	10.12	53.6
	1084	176	176	75.0	5.4	19.0	22.8	.90	7.7	26.0	54.2						24.0	9.82	50.0
	1085	170	170	77.0	5.4	17.0	22.1	.50	7.7	25.0	52.1						23.4	9.73	48.8
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.75 max	10 max	22 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

PACIFIC SEMICONDUCTORS, INC,

RESEARCH AND DEVELOPMENT DEPARTMENT

TRANSISTOR 25W-100MC - TYPE [redacted]

Box No. 23

DATE 6-4-63

OPERATOR AB and HF

PAGE 5 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CB} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o (OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION					POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W V_{CE} = 80V f = 100 Mc I_C = 600mA.		
												θ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	P_o	P_G	N
		V	V	µA	V	ratio	pf	V	Ω	W	%	°C/W	V	V	µA	ratio	W	db	%
	1086	178	178	116.0	5.4	25.0	23.0	.20	7.2	26.0	54.2						24.6	9.92	51.2
	1087	182	182	.22	5.3	32.0	23.2	.80	7.0	27.5	57.3						25.7	10.12	53.6
	1088	171	171	70.0	5.4	17.0	24.4	.30	7.0	25.4	52.9						24.0	9.82	50.0
	1089	170	170	.155	5.5	30.0	23.7	.40	6.5	25.6	53.4						25.0	10.00	52.1
	1090	172	172	100.	5.4	13.0	26.5	.40	7.5	27.6	57.5						26.7	10.28	55.6
	1091	182	182	4.60	5.4	14.0	22.6	1.00	6.5	24.0	50.0						24.0	9.82	50.0
	1092	180	180	125.0	5.4	14.0	24.0	.75	6.2	26.0	54.2						24.6	9.92	51.2
	1093	170	170	.42	5.5	35.0	21.8	.20	6.2	26.0	54.2						23.6	9.74	49.2
	1094	178	178	23.4	5.4	25.0	21.5	.20	6.5	27.0	56.3						26.1	10.19	54.4
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.75 max	10 max	25 min		2.5 max	170 min	180 min	200 max	9 min	25 min	10 min	

PACIFIC SEMICONDUCTORS, INC,

RESEARCH AND DEVELOPMENT DEPARTMENT

TRANSISTOR 2N4-100MC - TO5

Box No. 23

DATE 6-4-63

OPERATOR AB and HF

PAGE 5 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CE} = 80V	V_{CE} (SAT) @ I_C = 1.0A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o (OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION					POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W V_{CE} = 80V f = 100 Mc I_C = 600mA.		
												@ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	P_o	P_g	N
		V	V	μA	V	ratio	pf	V	Ω	W	%	°C/W	V	V	μA	ratio	W	db	%
	1086	178	178	116.0	5.4	25.0	23.0	.20	7.2	26.0	54.2						24.6	9.92	51.2
	1087	182	182	.22	5.3	32.0	23.2	.80	7.0	27.5	57.3						25.7	10.12	53.6
	1088	171	171	70.0	5.4	17.0	24.4	.30	7.0	25.4	52.9						24.0	9.82	50.0
	1089	170	170	.155	5.5	30.0	23.7	.40	6.5	25.6	53.4						25.0	10.00	52.1
	1090	172	172	100.	5.4	13.0	26.5	.40	7.5	27.6	57.5						26.7	10.28	55.6
	1091	182	182	4.60	5.4	14.0	22.6	1.00	6.5	24.0	50.0						24.0	9.82	50.0
	1092	180	180	125.0	5.4	14.0	24.0	.75	6.2	26.0	54.2						24.6	9.92	51.2
	1093	170	170	.42	5.5	35.0	21.8	.20	6.2	26.0	54.2						23.6	9.74	49.2
	1094	178	178	23.4	5.4	25.0	21.5	.20	6.5	27.0	56.3						26.1	10.19	54.4
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.75 max	10 max	25 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

PACIFIC SEMICONDUCTORS, INC,
RESEARCH AND DEVELOPMENT DEPARTMENT
TRANSISTOR 25W-100MC - 7[illegible]
[illegible] PA 36-009 MC 6[illegible]

Box No. 24
Copper-Ceramic Headers

DATE 6-4-63
OPERATOR AB and HF
PAGE 6 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CE} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o (OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION					POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W V_{CE} = 80V f = 100 Mc I_C = 600mA		
												@ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	P_o	P_G	N
		V	V	µA	V	ratio	pf	V	Ω	W	%	°C/W	V	V	µA	ratio	W	db	%
	1066	170	170	102.0	5.4	37.0	26.0	.50	6.2	26.0	54.2						26.6	10.27	55.4
	1067	165	165	107.0	5.4	14.0	24.8	.60	6.5	27.0	56.3						25.6	10.10	53.4
	1068	172	172	216.0	5.4	13.0	27.5	.95	6.5	29.0	60.4						26.6	10.27	55.4
	1069	170	170	.0025	5.5	40.0	24.9	.45	6.5	27.8	58.0						26.2	10.20	54.6
	1070	170	170	12.1	5.4	12.0	24.7	1.35	5.5	28.4	59.2						26.6	10.27	55.4
	1071	178	178	144.0	5.4	14.5	23.8	1.00	6.2	28.6	59.6						27.0	10.33	56.3
	1072	172	172	15.3	5.3	12.5	24.9	1.65	5.5	28.4	59.2						25.7	10.12	53.6
	1073	172	172	80.0	5.5	47.0	23.2	.35	6.5	27.8	58.0						26.4	10.24	55.0
	1074	174	174	10.5	5.5	18.0	24.0	1.95	6.7	27.4	57.1						25.6	10.10	53.4
LIMITS		170 min	170 min	100 max	[illegible] min	10 min	25 max	.95 max	10 max	25 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

PACIFIC SEMICONDUCTORS, INC,
RESEARCH AND DEVELOPMENT DEPARTMENT
TRANSISTOR 25W-100MC - TYPE
[redacted] PC 65753

Box No. 25
Copper-Ceramic Headers

DATE 6-4-63
OPERATOR AB and HF
PAGE 7 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CB} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o (OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION @ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W, f = 100 Mc, V_{CE} = 30V, I_C = 600mA		
																	P_o	P	N
		V	V	μA	V	ratio	pf	V	Ω	W	%	°C/W	V	V	mA	ratio	W	db	%
	1075	172	172	166.0	5.5	30.0	24.4	2.50	6.5	24.6	51.2						23.6	9.74	49.2
	1104	170	170	.46	5.3	10.5	25.0	.95	7.0	28.7	59.5						26.7	10.28	55.6
	1105	170	170	.014	5.4	13.0	24.8	.45	6.5	28.4	59.2						26.6	10.27	55.4
	1106	164	164	22.8	5.4	37.0	25.2	.45	6.2	26.7	55.6						26.6	10.27	55.4
	1107	164	164	100.	5.4	33.0	25.6	.45	6.7	27.0	56.3						26.5	10.25	55.2
	1108	170	170	200.	5.4	52.0	25.2	.25	8.2	27.1	56.9						27.4	10.40	57.1
	1109	172	172	72.5	5.2	175.	23.5	.20	8.2	27.0	56.3						26.7	10.28	55.6
	1110	180	180	30.0	5.3	17.0	24.2	.45	6.2	29.6	61.7						28.1	10.51	58.6
	1111	170	170	90.0	5.3	17.0	26.1	.30	7.2	28.0	58.4						27.6	10.43	57.5
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.5 max	10 max	22 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

PACIFIC SEMICONDUCTORS, INC,
RESEARCH AND DEVELOPMENT DEPARTMENT
TRANSISTOR 25W-100MC - TSW
[redacted]

Box No. 26
Copper-Ceramic Headers

DATE 6-10-63
OPERATOR HF
PAGE 8 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CB} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o (OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION @ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W f = 100 Mc V_{CE} = 80V I_C = 600mA		
																	P_o	P_G	N
		V	V	μA	V	ratio	pf	V	Ω	W	%	°C/W	V	V	μA	ratio	W	db	%
	1112	170	170	32.0	5.4	14.0	25.1	.95	6.2	27.5	57.3						26.5	10.25	55.2
	1113	170	170	.003	5.4	34.	26.	.35	5.5	27.4	57.1						27.1	10.35	56.5
	1114	170	170	66.	5.4	30.0	25.	.20	6.2	28.0	58.4						27.6	10.43	57.5
	1115	164	164	25.2	5.3	60.0	24.8	.38	7.5	26.0	54.2						26.5	10.25	55.2
	1116	170	170	.045	5.4	10.0	24.6	1.5	5.2	28.0	58.4						26.6	10.27	55.4
	1117	174	174	5.40	5.3	11.5	24.5	1.55	5.2	28.7	59.8						27.6	10.43	57.5
	1118	164	164	56.0	5.5	31.5	25.0	.20	7.5	25.6	53.4						26.0	10.17	54.2
	1119	170	170	600.	5.4	32.0	24.4	.15	8.0	27.6	57.5						28.0	10.49	58.2
	1120	174	174	3.0	5.5	13.0	24.5	.40	6.25	28.4	59.2						27.8	10.46	58.0
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.75 max	10 max	25 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

PACIFIC SEMICONDUCTORS, INC,

RESEARCH AND DEVELOPMENT DEPARTMENT

TRANSISTOR 25W-100MC - TYPE [redacted]

[redacted] SC 05723

Box No. 27

Copper-Ceramic Headers

DATE 6-11-63

OPERATOR HF

PAGE 9 OF 9

RUN NO.	UNIT NO.	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	V_{EBO} @ I_E = 5 mA	h_{FE} @ V_{CE} = 5V I_C = 600 mA	C_{ob} @ V_{CE} = 80V	V_{CE} (SAT) @ I_C = 1.5A I_B = 300 mA	r'_b @ V_{CE} = 80V I_C = 100 mA	P_o(OSC) @ V_{CE} = 80V I_C = 600mA f = 100mc		GROUP B INSPECTION					POWER GAIN NEUT. COMMON EMITTER P_{in} = 2.5W f = 100 Mc V_{CE} = 80V I_C = 600mA		
												θ J-C	V_{CBO} @ I_C = 100 mA	V_{CES} @ I_C = 100 mA	I_{CES} @ V_{CE} = 80V	h_{FE} @ V_{CE} = 5V I_C = 600 mA	P_o	P_G	N
		V	V	µA	V	ratio	pf	V	f	W	%	°C/W	V	V	µA	ratio	W	db	%
	1121	164	164	405.	5.4	44.0	25.8	.15	7.5	26.2	54.4						26.8	10.30	55.9
	1122	162	162	370.	5.4	28.0	29.5	.20	6.75	25.6	53.4						26.6	10.27	55.4
	1123	170	170	73.5	5.4	19.0	26.1	.15	7.5	28.0	58.4						28.0	10.49	58.4
LIMITS		170 min	170 min	100 max	5 min	10 min	25 max	.75 max	10 max	25 min		2.5 max	170 min	170 min	200 max	9 min	25 min	10 min	

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